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MODEL 1626
SAFETY PRACTICES

Personnel assigned to the operation or maintenance of the Model 1626 Microwave Synthesizer are encouraged to review the safety practices given in this section. These are recommended procedures which may prevent a serious accident, save a life, or protect the instrument from damage.

Whenever the safety of operating or maintenance personnel is involved, special safety instructions are inserted in the text as "WARNINGS." Instructions concerning the safety of equipment are inserted as "CAUTIONS." These notations are discussed in greater detail at the end of this section.

The following recommended procedures should be understood and applied during any phase of operation or maintenance of this equipment:

CHASSIS GROUNDING

Prior to applying power to Model 1626, determine that the internal protective power ground is connected to the protective ground conductor of the power cord. This ground, in turn, must be connected through the external power cord to the grounded power outlet. (Verify ground continuity using an ohmmeter, with power totally removed from the instrument.)

a. Any interruption of the protective ground conductor, inside or outside of the Model 1626 instrument, could create a potentially hazardous condition due to possible (chassis) voltage differences between this and other equipments. When Model 1626 is connected into a system with other units, all power grounds should connect through a common bus to optimize circuit breaker response in the event of electrical failure. Intentional interruption of the grounding system by the use of two-wire plug adapters or two-wire extension cords must be considered an unsafe practice.

b. Whenever it is determined that the protective ground system has been impaired, the equipment must be made inoperative or be secured against inadvertent operation until the deficiency is corrected.

KEEP AWAY FROM LIVE CIRCUITS

Operating and maintenance personnel are cautioned against using the Model 1626 with top and/or bottom cover panels removed and power applied, unless directed to do so by a specific instruction manual procedure (troubleshooting, calibration, etc).

a. Under certain conditions, dangerous potentials may still exist when power is removed from the instrument due to charges retained by capacitors. To avoid injury, always remove power; then, discharge or ground any large capacitors prior to replacing components or making repairs.

b. To avoid potential damage to Model 1626, always remove power from the instrument before extracting or inserting any circuit boards and/or discrete components.

c. Troubleshooting, repair, or adjustments of the Model 1626 with power applied to the circuits should be minimized whenever possible. However, when instruction manual procedures so dictate, these should be performed only by skilled technical persons who are aware of the various hazards involved.

DO NOT SERVICE OR ADJUST ALONE

Under no circumstance should any person service or adjust equipment unless in the presence of another person who is capable of rendering first aid/resusitation services in the event of accident.

DEFECTIVE PARTS REPLACEMENT

To avoid possible damage or degrading of instrument performance, technical personnel are cautioned to replace defective components only with new factory replacement items; or, in certain cases, cross-referenced, direct-substitute items. Be certain that only the correct power fuse with required rating (voltage/current) and specified type (fast blow, slow blow, etc) is used for replacement purposes. The use of repaired fuses or short-circuiting of the fuseholder is considered an unsafe practice.

SAFETY SUMMARY

The following safety symbols are used on the Model 1626 instrument and/or in this manual:

Instruction manual symbol: the instrument will be marked with this symbol when it is necessary for the user to refer to the instruction manual.

Indicates hazardous voltages.

Indicates earth (ground) terminal.

WARNING

The **WARNING** sign denotes a personnel hazard. It calls attention to a procedure or practice, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a **WARNING** sign until the indicated conditions are fully understood and met.

CAUTION

The **CAUTION** sign denotes an instrument hazard. It calls attention to an operating procedure or practice, which, if not correctly performed or adhered to, could result in damage to, or destruction of part or all of the instrument. Do not proceed beyond a **CAUTION** sign until the indicated conditions are fully understood and met.

Warnings and Cautions appearing in the text of this instruction manual are repeated here for review and emphasis by personnel operating or maintaining this instrument .

WARNING

The YIG Drivers supply high currents through the fuse bank shown in figure 2-2. These currents can cause severe burns if inadvertently shorted.

Page 2-1.

WARNING

The synthesizer weighs approximately 26.3 kg (58 lbs.). Be sure to provide adequate rack-shelf mounting for the unit and exercise care when lifting to avoid personal injury.

Page 2-3.

CAUTION

Damage may be sustained by the Model 1626 if greater than +20 dBm is impressed on the RF OUT ⑭ connector.

Damage may also be sustained by the power meter if greater than +20 dBm is applied to the EXT POWER METER INPUT ⑪.

Page 3-4.

CAUTION

Before removing or inserting any PCB assembly, turn off the instrument power and allow at least 30 seconds for the power supply to discharge, to prevent damage to the subject PCB assemblies. Use care in the removal and reinsertion of the PCB assemblies to avoid any mechanical damage.

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CHAPTER 1
GENERAL INFORMATION

1-1. INTRODUCTION

1-2. This instruction manual contains information relating to installation, operation, maintenance, and calibration of the Systron Donner Model 1626 Microwave Synthesizer. Figure 1-1 shows the Model 1626 and the supplied accessories.

1-3. The information contained in this instruction manual is divided into front matter and seven descriptive chapters indicated in the following format:

Front Matter: includes the title page, proprietary rights statement, list of effective pages, record of changes, table of contents, list of figures, list of tables, and safety practices information.

Chapter 1 - General Information: contains a general description of Model 1626 including specifications, accessories supplied, and safety practices.

Chapter 2 - Installation: describes unpacking and inspection, installation criteria, initial turn-on/confidence checks, IEEE Std 488 GPIB system interconnection, and preparation for reshipment.

Chapter 3 - Operation: provides descriptions of front- and rear-panel controls, indicators, and connectors located on Model 1626. It also includes instrument operating procedures, supplemented by IEEE Std 488 GPIB programming characteristics.

Chapter 4 - Principles of Operation: contains a detailed functional/circuit description of Model 1626 which will assist technical personnel in the performance of troubleshooting and/or calibration procedures.

Chapter 5 - Maintenance: describes the steps required for routine maintenance, inspection, alignment, and performance verification.

Chapter 6 - Replaceable Parts: are listed in this chapter along with parts ordering information, and a manufacturer's code-to-name index.

Chapter 7 - Drawings: provides technical personnel with requisite schematic and component locator diagrams for maintenance and troubleshooting of Model 1626.

1-4. EFFECTIVITY OF MANUAL

1-5. Information contained in this instruction manual is code-dated at the bottom of each page. A summary of these code dates is given in the List of Effective Pages provided in the front matter of this manual. Instrument changes, which occur after the printing of this manual, will be documented by change supplements to be inserted into the front of future publications. Change supplement information may also include the correction of errors which were not yet determined at the date of this publication.

1-6. DESCRIPTION

1-7. The Model 1626 Microwave Synthesizer is a portable, self-contained, 0.1 to 26.0 GHz synthesized signal source with full generator capabilities. The microwave output may be swept, leveled, attenuated, modulated, and phase locked to an internal or external 1 MHz reference. Both the frequency and power level of the output signal are continuously displayed on a built-in digital frequency meter and digital power meter. All controls, inputs, outputs and displays, with the exception of the power cord, line fuses, remote programming connector, address switches and pen lift, are accessed from the front panel.

1-8. RF Output

1-9. The output frequency is settable from 0.1 to 26 GHz in 1 MHz steps with CW/START, GHz leverwheel switches on the front panel.

1-10. Sweep Control

1-11. The output rf may be swept upward 10 MHz to 9.999 GHz from a fixed CW/START, GHz frequency by setting the ΔF, GHz leverwheel switches from 0.010 to 9.999 GHz. The two sweep rates, 1 kHz or .1 kHz, are selected with two front-panel pushbuttons. A momentary pushbutton is also provided for manually incrementing the CW/START, GHz frequency in single 1 MHz steps. Another momentary pushbutton manually resets the sweep back to the CW/START, GHz frequency. The SWEEP OUT BNC connector on the front panel supplies a 0 to 10 V ramp for controlling external devices.

1-12. Output Level, Power Meter

1-13. A built-in microwave digital power meter continuously displays the rf output level in dBm. The INT full display range is +19 to −99 dBm. This meter will also measure the power of an external microwave source from +10 to −30 dBm. Attenuation of the output is provided by two decade step attenuators: these 10 to 90 dB and 0 to 9 dB attenuators provide a full 0 to 99 dB attenuation range. A LEVEL vernier control provides a leveled +5 dBm rf reference output. This control also provides unleveled 0 to 10 dB continuous overrange up to the maximum available output.

1-14. Modulation

1-15. Model 1626 may be amplitude modulated both internally and externally. Two types of internal

amplitude modulation may be selected: square wave or pulse. The 1 kHz square wave modulation provides rf bursts at 50% duty cycle. The pulse modulation provides a variable duration rf burst from 0.1 to 10 μs.

The amplitude modulation may be removed by selecting OFF. An external sync TTL output signal is provided on the MOD input BNC connector when using internal modulation. When external modulation is selected, the MOD input BNC connector accepts an external TTL-compatible modulation signal, either leading- or trailing-edge triggered.

1-16. Reference

1-17. The internal 1 MHz reference is available on the 1 MHz REF BNC as an output when INT is selected and the same BNC will accept an external 1 MHz signal as a reference input for the synthesizer when EXT is selected.

1-18. SPECIFICATIONS

1-19. The specifications for the Model 1626 Microwave Synthesizer are listed in Table 1-1. Any acceptance test or calibration procedure will use these specifications as a tolerance guide.

Table 1-1. Specifications

PERFORMANCE LIMITS
Frequency
Frequency Range: 100 MHz to 26 GHz.
Frequency Resolution: 1 MHz.
Frequency Aging Rate: 1 ppm/year.
Reference Output: 1 MHz, 2 V p-p into 50 Ω.
External Reference Input: 1 MHz, 1 V rms.
Residual FM: ≤ 1 kHz or 0.0001% of frequency, p-p (30 Hz to 10 kHz bw).
Spectral Purity
Harmonics and Subharmonics: < −55 dBc.
Spurious (nonharmonically related): < −55 dBc at >10 kHz offset.
RF Output
Output Level: +5 dBm leveled, ≥ +5 dBm typical unleveled.
Leveling Accuracy: ±1 dBm, 0.1 to 18 GHz. ±2 dBm, 18 to 26 GHz.

Table 1-1. Specifications (Cont'd)

Output Level Display: 3-1/2 digit LED display, 0.1 dB resolution. +19 dBm to −99 dBm.
Output Attenuator: 90 dB, in 10 dB steps; 9 dB, in 1 dB steps.
Level Adjust: 0 to 10 dB continuous overrange control up to maximum available power.
Output Connector: WPM-3 (SMA compatible).
Output Impedance: 50 Ω nominal.
Power Measurement
Frequency Range: 100 MHz to 26 GHz.
Input Level: +10 dBm to −30 dBm.
Accuracy: ±1 dB +10 dBm to −10 dBm ±2 dB −10 dBm to −30 dBm
Measurement Display: 3-1/2 digit LED display 0.1 dB resolution.
Input Connector: WPM-3/SMA compatible.
Input Impedance: 50 Ω nominal.
Modulation
Pulse Modulation Internal Rate: Fixed 1 kHz and variable 100 Hz to 50 kHz.
Duration: CAL pulse position, 1 μs calibrated; or variable pulse width, 0.1 μs to 10 μs.
External Input: 100 Hz to 50 kHz prf, 0.1 μs min. pw, TTL levels.
Sync Output: Modulation waveform, TTL levels.
ON/OFF Ratio: ≥ 30 dB.
Rise/Fall: ≤ 25 ns.
Pulse Overshoot/Undershoot: 2 dB maximum, settles to within ±1 dB in 100 ns.
Sweep
Range: Minimum 10 MHz, maximum 9.999 GHz, selectable in 1 MHz increments over full range (no band limits).
Frequency Step Size: 1 MHz.
Step Rate: 1 kHz, 100 Hz or single step.
Sweep Out: 10 V ramp for any sweep width >10 MHz.
Pen Lift: 1 V min., transistor switched-to-ground during retrace.

Table 1-1. Specifications (Cont'd)

General
Operating Temperature: 10° to 40°C.
Weight: 58 lbs (26.3 kgm).
Dimensions: W × D × H; 16.75" (425 mm) × 24.25" (616 mm) × 5.25" (133 mm).
Power: 100/115 and 200/230 V ac ±10%, 48 to 400 Hz, 250 W.
Programmability: IEEE Std 488 Interface. This provides remote control of frequency, sweep range, sweep rate, pulse/square-wave modulation, 1 dB step attenuator, and output level adjust.

1-20. SUPPLIED ACCESSORIES

1-21. Included with Model 1626 Microwave Synthesizer are the accessories listed in table 1-2.

1-22. SAFETY PRACTICES

1-23. Prior to operation or maintenance of Model 1626, technical personnel are encouraged to review the safety practices section located in the front matter of this manual. Removal of the top or bottom cover while the synthesizer is operating exposes personnel to possible contact with high voltage and high current sources. Always remove main power to the instrument when servicing and only allow qualified personnel to maintain this instrument.

Table 1-2. Supplied Accessories

Description	Part Number
Carrying Handle, integral to instrument; Qty. 2.	067440
Line Cord, 2 meter, 3 × 18 ga, Rtang; Qty 1.	117644
Extender PC card, 44-pin (22-pin dual inline); Qty 2.	06738301
Extractor, PC card; Qty 1.	053948
Rack-Mount Kit, consisting of the following:	075906
Flange, rack mount, right; Qty 1.	067448
Flange, rack mount, left; Qty 1.	067504
Screw, PHMS 10-32 × 5/8; Qty 4.	10064410
Washer, split-lock #10; Qty 4.	100714

CHAPTER 2

INSTALLATION

2-1. INTRODUCTION

2-2. This chapter outlines the procedures for initial inspection and installation of the Model 1626 Microwave Synthesizer. The subject matter includes receiving inspection, installation criteria, initial turn-on/confidence checks, and IEEE Std 488 GPIB system interconnection. Instructions concerning preparation for reshipment are included at the end of this chapter.

2-3. RECEIVING INSPECTION

2-4. Prior to accepting the unit from the shipper, inspect the condition of the shipping container for any indication of freight damage. Any sign of such damage must be noted by both the shipper and receiver and should be reported to the insurance investigator.

2-5. Immediately following removal of the unit from the shipping carton, inspect for possible physical damage incurred during shipment. Check surfaces for scratches or dents and note the condition of knobs and connectors. Should any damage be detected, notify your nearest Systron Donner representative - DO NOT USE THE INSTRUMENT UNTIL INSTRUCTED TO DO SO BY THE REPRESENTATIVE.

2-6. POWER REQUIREMENTS

2-7. The Model 1626 is equipped with a detachable three-conductor power cord that automatically grounds the chassis when a matching power receptacle is employed. If an adapter plug is used, the chassis ground must be connected wherever the power cord is mated to a two-terminal outlet.

2-8. The synthesizer operates over the line voltage range of 100/115 or 200/230 V ac, ±10%, at 48 to 400 Hz. Power consumption is 250 W. An internal Molex connector, J1, accepts one of four different jumpered plugs (P1) to match existing line voltage conditions. See figure 2-1. Plug P1 jumper pins are listed in table 2-1 and are silk screened on the inside of the card cage cover.

2-9. Fuses

2-10. The Model 1626 is shipped with a 3 A, 3AG slow-blow fuse (main) for 100/115 V ac nominal operation. Should 200/300 V ac nominal operation be employed, the standard 3 A, 3AG slow-blow fuse should be replaced with a 1.5 A, 3AG slow-blow fuse to adequately protect the instrument. Power supply output currents to the microwave assembly are also fused. The value of these fuses is given in table 2-2. Fuse locations are indicated in figure 2-2.

WARNING

The YIG drivers supply high currents through the fuse bank shown in figure 2-2. These currents can cause severe burns if inadvertently shorted.

NOTE

An automatic resetting, over-temperature switch, A1S1, is incorporated into Model 1626 which removes ac line power from the instrument if internal overheating occurs. See figure 2-2 for location and paragraph 3-6, NOTE for details.

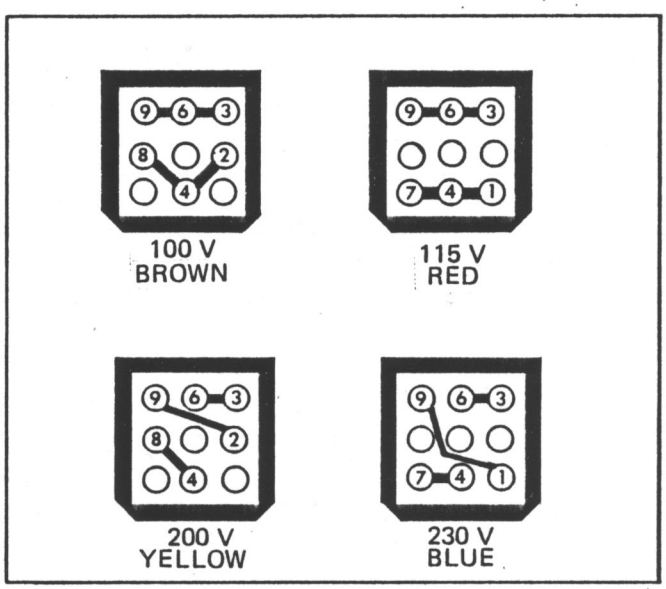


Figure 2-1. Power-Line Range Selector, Plug P1

2-11. LOCATION SITE

2-12. For installation purposes, an outline-dimension/rack-mounting diagram is provided in figure 2-3 to assist Model 1626 installation personnel. The rear panel must remain unobstructed (4" to 6" clearance) while the synthesizer is operating to allow proper cooling; also, access to the rear panel-mounted fuseholder, address switches, GPIB interface connector, and power cord is necessary. Periodic cleaning of the air filter also requires access to the rear panel.

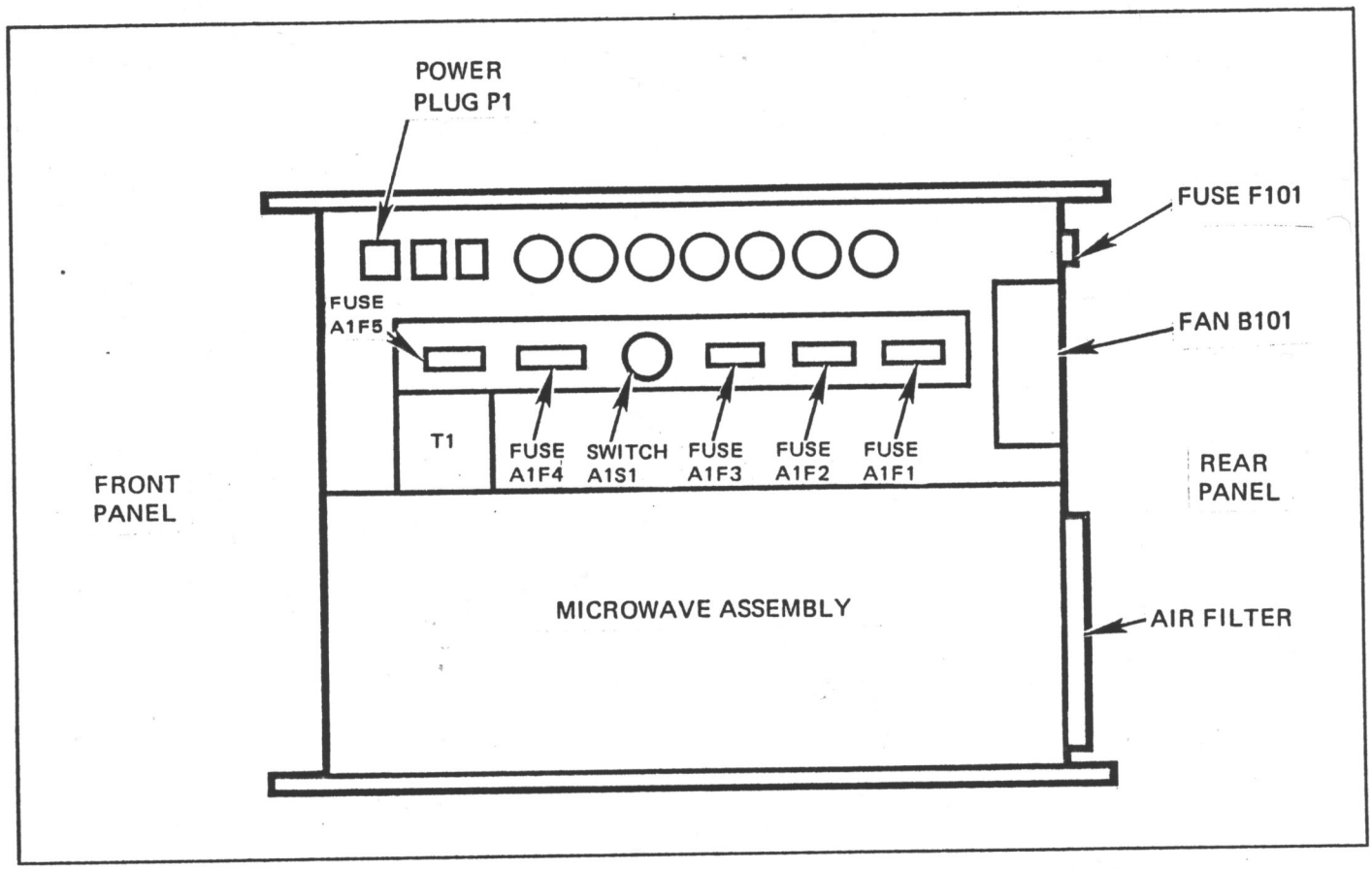


Figure 2-2. Plug P1 and Fuse Locations, Top View, Model 1626

Table 2-1. Power Line Jumper Plug Pins, P1

Voltage (Nominal)	Jumper Pins	Wire Color	SD P/N
100	9-6-3, 8-4-2	Brown	07575701
115	9-6-3, 7-4-1	Red	07575702
200	6-3, 9-2, 8-4	Yellow	07575703
230	6-3, 9-1, 7-4	Blue	07575704

Table 2-2. Instrument Fuses

Ref	Description	Mfg. & P/N	SD P/N
F101	3 A 3AG S.B. (100/115 V operation)	75915 / 313003	106910
F101(Alt)	1.5 A 3AG S.B. (200/230 V operation)	75915 / 31301.5	100591
A1F1	1.5 A 3AG M.B.	75915 / 31201.5	100588
A1F2	1.5 A 3AG M.B.	75915 / 31201.5	100588
A1F3	1.5 A 3AG M.B.	75915 / 31201.5	100588
A1F4	1.5 A 3AG M.B.	75915 / 31201.5	100588
A1F5	1.5 A 3AG M.B.	75915 / 31201.5	100588

2-13. Bench Mounting

2-14. Model 1626 may be installed on a bench with clearance provided for the rear panel connectors. See figure 2-3. The air intake and exhaust ports, located on the rear panel, must remain unobstructed to allow adequate cooling of the instrument.

2-15. The instrument is supplied with a swing -down-type bail mounted on the front of the bottom cover. When extended, this stand will tilt-up the front panel of Model 1626 to a comfortable viewing angle.

2-16. Rack Mounting

2-17. The instrument is shipped with two rack-mounting brackets, and four #10-32 × 5/8 screws. To assemble, remove the two forward bottom-row cover screws on the right and left sides of the unit. See figure 2-3. Attach the right- and left-hand rack-mounting bracket to each side of the cabinet with the supplied hardware, as shown.

WARNING

The synthesizer weighs approximately 26.3 kg (58 lbs). Be sure to provide adequate rack-shelf mounting for the unit and exercise care when lifting to avoid personal injury.

2-18. Optional equipment rack slides are recommended when rack mounting the Model 1626. The slides are available from the factory as a standard accessory. Follow the mounting procedure shown in figure 2-3 for rack mounting, then mount the rack slides, as shown. When completed, check the installation to be certain that all top-cover mounting screws are clear for removal should servicing be required.

Rack-Mounting Slides and Hardware Kit
SD No. 067834

2-19. Operating Environment

2-20. The operating temperature for Model 1626 is 10° to 40°C with a relative humidity of < 95%. The maximum altitude is < 4572m (15,000 ft.).

2-21. INITIAL TURN-ON

2-22. This procedure verifies that instrument damage has not occurred during transit and that the unit is operative. Prior to performing the initial turn-on procedure, become familiar with the synthesizer controls as described in paragraph 3-3 Controls, Connectors, and Indicators.

a. Utilize the following step procedures to initially check the operation of Model 1626 (full-performance test procedures appear in chapter 5):

1. Check the internal power jumper plug, P1, for the proper line-voltage operating range and connect the ac power cord to the appropriate line power source.
2. Actuate the LINE switch to the ON position. The display should illuminate. Press the DISPLAY TEST button to verify that all segments of the LED displays operate and the LOCK, LEVEL, and REMOTE LED indicators illuminate.
3. Select MODULATION, OFF; 1 MHz REF, INT; CW; POWER METER, INT; ATTENUATION, 0,0; LEVEL, LEVELED.
4. Select a frequency with the CW/START, GHz leverwheel switches between 0.1 and 26.0 GHz.
5. Within a one half-hour warm-up period the LOCK and LEVEL LED lamps will illuminate green indicating that the rf output is phase locked with the internal or external reference; also, the amplitude of the microwave output is leveled. Red indicates an unlocked or unleveled condition. The FREQUENCY, GHz and POWER METER, dBm displays will indicate the frequency and power level of the RF OUT connector.
6. Setting the two ATTENUATION controls will attenuate the output power from 0 to -99 dB. Full internal display range of POWER METER, dBm readout is +19 to −99 dBm.
7. The POWER METER, EXT COMP switch position may be used to measure the rf output power by externally coupling the RF OUT connector to the POWER METER, INPUT connector using an eight-inch piece of semi-rigid 141 cable. This cable has at least 0.8 dB/ft loss so the power readings at 26 GHz will be slightly lower for external measurement.
8. Select 1 kHz or .1 kHz SWEEP pushbutton and set the ΔF, GHz leverwheel switches to any desired sweep range (step) from .010 to 9.999 GHz. The FREQUENCY, GHz display will indicate the frequency set in the CW/START, GHz leverwheels while being swept at the 1 kHz or 0.1 kHz rate (up to the ΔF, GHz limit and then returning to the CW/START, GHz frequency). A single sweep is selected by pressing the 1 STEP pushbutton. RESET pushbutton sets the rf output back to the CW/START, GHz frequency.

2-23. Mating Connectors

2-24. The RF OUT and POWER METER INPUT are SMA-compatible, 50 Ω coaxial connectors. All other connectors are 50 Ω coaxial-type BNC, with the exception of a 24-pin GPIB remote programming connector and the power cord receptacle.

2-25. GPIB SYSTEM CONNECTION, REMOTE PROGRAMMING

2-26. The General Purpose Interface Bus (GPIB) permits data bus control of Model 1626 according to the IEEE Standard Digital Interface for Programmable Instruments (IEEE Std 488-1978).

2-27. To implement the GPIB, a 24-pin metric-dimensioned connector and a 5-digit address selector switch are installed on the rear panel of the synthesizer.

2-28. A detailed description of the GPIB interface operation is given in chapter 3 of this manual. Table 2-3 provides the pin assignments for the rear panel GPIB 24-pin connector.

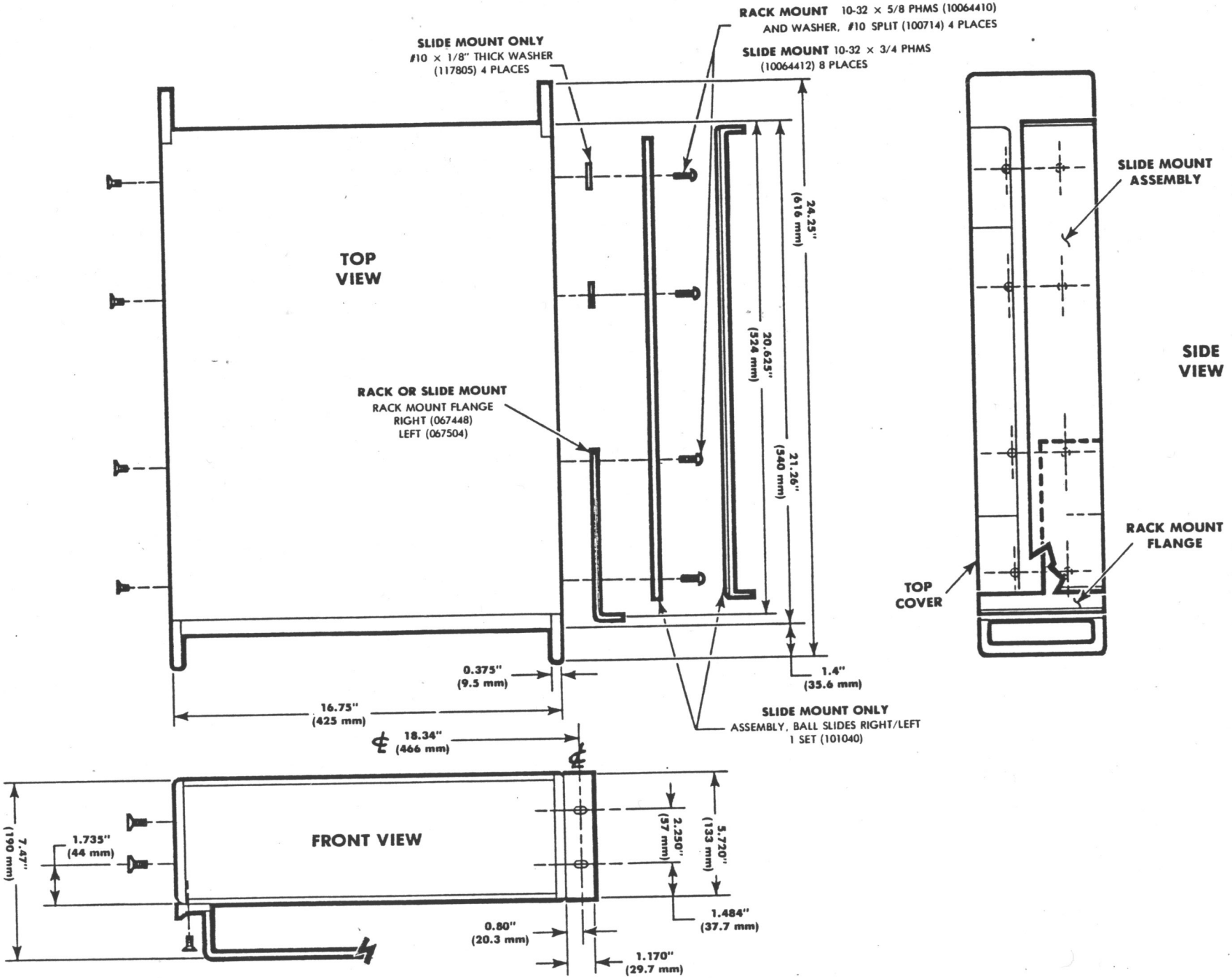


Figure 2-3. Outline Drawing and Rack/Slide Mounting Details

Table 2-3. GPIB Interface Connector

Pin Number	IEEE Std 488 Mnemonic
1	DI01
2	DI02
3	DI03
4	DI04
5	EOI (Inactive)
6	DAV
7	NRFD
8	NDAC
9	IFC
10	SRQ (Inactive)
11	ATN
12	GND (Shield)
13	DI05
14	DI06
15	DI07
16	DI08 (Inactive)
17	REN
18	GND (Return for 6)
19	GND (Return for 7)
20	GND (Return for 8)
21	GND (Return for 9)
22	GND (Return for 10)
23	GND (Return for 11)
24	GND (Logic)

LEVELS:
TTL compatible, true (1) state is 0.0 to +0.8 V dc; false (0) state is +2.5 to +5.0 V dc.

MATING CONNECTOR:
Amphenol 57-30240.

MATING CABLES:
IEEE Std 488 Cable - 1 meter length
SD No. 011707601
IEEE Std 488 Cable - 2 meters length
SD No. 011707602
IEEE Std 488 Cable - 3 meters length
SD No. 011707603

2-29. PREPARATION FOR RESHIPMENT

2-30. When Model 1626 is to be repackaged for shipment, use the original packing materials or package in accordance with MIL-P-116 and MIL-E-17555E specifications.

a. Repackage the instrument using the following step procedures:

1. Attach an identification tag to the Model 1626 indicating model number, serial number, name and address of instrument owner, and a summary of the service or repairs required.
2. Wrap the instrument in heavy paper or plastic prior to placing it in the shipping container.
3. Select a strong carton or wooden box as a shipping container.
4. Use an adequate layer of shock-absorbing material on all six sides of the unit. Protect the instrument front panel with additional layers of cardboard. Ensure that no movement of the assembly is evident within the container.
5. Seal the shipping container with strong tape or metal bands and attach a packing list to the outside surface.
6. Mark the shipping container "FRAGILE-DELICATE INSTRUMENT" and attach the appropriate handling symbols to ensure reasonable care in transit.
7. Be certain that all correspondence relating to the service or repair of this instrument includes the information contained on the instrument identification tag.

CHAPTER 3

OPERATION

3-1. INTRODUCTION

3-2. This chapter describes the Model 1626 Microwave Synthesizer operating procedures. The instrument controls, connectors, and indicators are described in tabular form and are indexed to match the annotated items of the front and rear panels.

3-3. CONTROLS, CONNECTORS, AND INDICATORS

3-4. The various controls, connectors, and indicators are described in table 3-1, Front Panel, and table 3-2, Rear Panel. Figures 3-1 and 3-2 provide indexed locations of each item.

NOTE

The operational capabilities of Model 1626 are described throughout this chapter in accordance with verifiable "Performance Limit" characteristics given in table 1-1, Specifications. Frequency and sweep select capabilities, however, extend beyond the range imposed by these specifications.

Table 3-1. Front Panel, Model 1626

Index	Name	Function
1	LINE, ON-OFF (toggle switch)	Switch turns the synthesizer main power on and off.
2	MOD (BNC connector)	Connector allows an external TTL-compatible 1 kHz squarewave or pulse signal to AM modulate the output rf signal 30 dB when MODULATION ㉕ selector is set to EXT. When MODULATION ㉕ selector is set to ⎍ (pulse) or ⎍⎍ (squarewave), this BNC connector provides an output of the internal modulation.
3	1 MHz REF, EXT (BNC connector)	Connector outputs internal 1 MHz reference signal when INT ④ is selected. The connector also accepts an external 1 MHz reference signal when EXT ④ is selected.
4	1 MHz REF, INT-EXT (toggle switch)	Switch selects either internal (INT) or external (EXT) 1 MHz reference.
5	CW (pushbutton switch)	Pushbutton activates the continuous wave, nonswept operating mode.
6	SWEEP, STEP RATE, 1 kHz (pushbutton switch)	Pushbutton activates sweep mode at a 1000 Hz step rate. The ΔF, GHz ⑳ leverwheel switches set sweep range and CW/START, GHz ㉒ leverwheel switches set start frequency.
7	SWEEP, STEP RATE, .1 kHz (pushbutton switch)	Pushbutton activates sweep mode at a 100 Hz step rate. The ΔF, GHz ⑳ leverwheel switches set sweep range and CW/START, GHz ㉒ leverwheel switches set start frequency.
8	SWEEP, 1 STEP (momentary pushbutton switch)	Pushbutton activates a single step when in SWEEP mode ⑥, ⑦.
9	SWEEP RESET (momentary pushbutton switch)	Pushbutton resets the sweep back to CW/START, GHZ ㉒ frequency.
10	SWEEP OUT (BNC connector)	BNC connector provides a 0 to 10 V (per sweep) output ramp for all sweep modes, regardless of the sweep size.

Table 3-1. Front Panel, Model 1626 (Cont'd)

Index	Name	Function
11	POWER METER, INPUT (SMA connector)	SMA connector accepts rf input to the internal digital POWER METER, dBm ⑱ when either EXT or EXT COMP is selected with POWER METER ⑲ switch. DO NOT EXCEED +20 dBm MAXIMUM INPUT.
12	ATTENUATION, −10 dB STEP (rotary selector switch)	Ten-step selector attenuates RF OUT ⑭ signal in 10 dB steps to a maximum of 90 dB.
13	ATTENUATION, −1 dB STEP (rotary selector switch)	Ten-step selector attenuates RF OUT ⑭ signal in 1 dB steps to a maximum of 9 dB.
14	RF OUT (SMA connector)	Synthesized 0.1 to 26 GHz microwave signal is available on this 50 Ω output connector. DO NOT EXCEED +20 dBm MAXIMUM REVERSE INPUT.
15	LEVEL, LEVELED-INCREASE, (rotary control with detent)	LEVELED detent position on this control is the calibrated level mode so that RF OUT ⑭ remains at +5 dBm with no attenuation dialed up. When rotated clockwise toward the INCREASE position, this control will unlevel the RF OUT ⑭ signal and increase the level above +5 dBm.
16	LOCK (green/red indicator)	Lamp illuminates green when output rf is phase locked with the internal or external reference, and illuminates red when output rf is not phase locked.
17	LEVEL (green/red indicator)	Lamp illuminates green when the output rf is leveled, and illuminates red when the output rf is unleveled.
18	POWER METER, dBm (LED display)	LEDs display power level in dBm of the internal or external rf, with 0.1 dBm resolution.
19	POWER METER, INT, EXT, EXT COMP (toggle switch)	When set to INT position, POWER METER dBm ⑱ displays signal power level at the RF OUT ⑭ connector. When EXT or EXT COMP is selected, POWER METER, dBm ⑱ displays power level of the signal applied to the INPUT ⑪ connector.
20	ΔF, GHz (leverwheel rotary switches)	Leverwheel switches are settable from 0.010 to 9.999 GHz by moving the lever up or down on each switch. This sets frequency width of the sweep when a sweep mode other than CW ⑤ is selected.
21	FREQUENCY METER, GHz (LED display)	LEDs display the signal frequency appearing at the RF OUT ⑭ connector.
22	CW/START, GHz (leverwheel rotary switches)	Leverwheel switches are settable from 00.100 to 26.000 GHz by moving the lever up or down on each switch. This sets the fixed output rf frequency on RF OUT ⑭ connector, or the start frequency for sweep mode of operation.
23	DISPLAY TEST (momentary pushbutton switch)	Test switch activates all segments of the display when pressed.
24	REMOTE (red LED indicator)	Lamp illuminates red when the synthesizer is operated from the IEEE Std 488 GPIB.

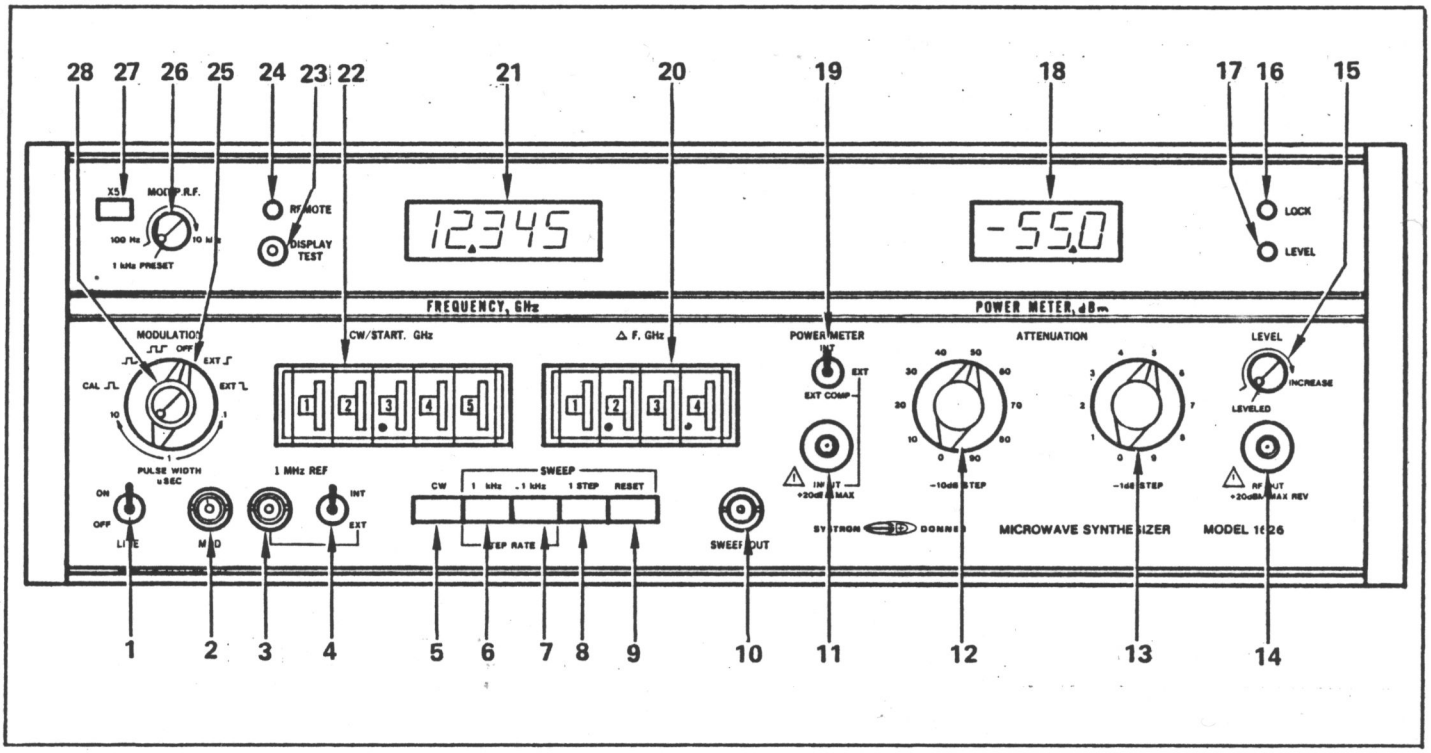


Figure 3-1. Front Panel, Model 1626

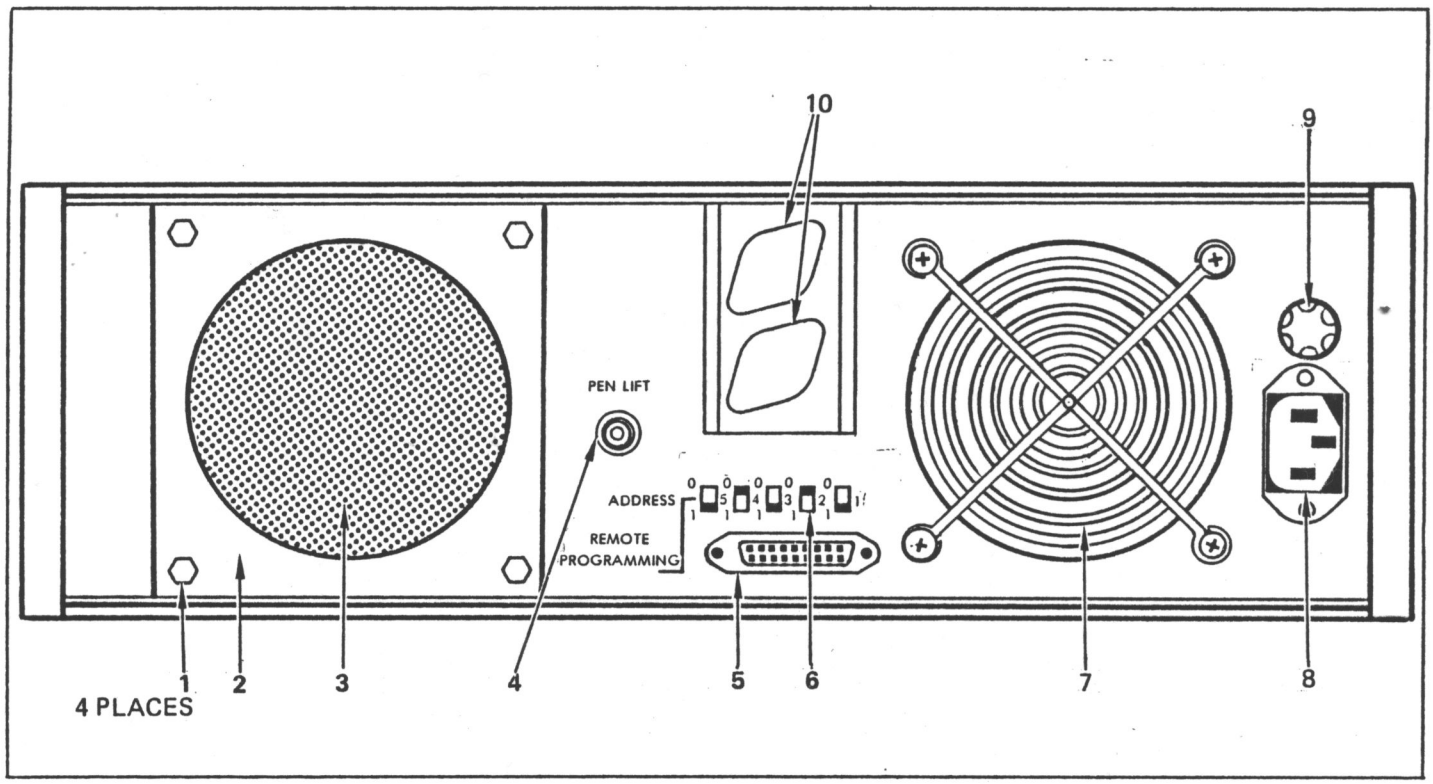


Figure 3-2. Rear Panel, Model 1626

Table 3-1. Front Panel, Model 1626 (Cont'd)

Index	Name	Function
25	MODULATION CAL ⎍, ⎍, ⎍⎍, OFF, EXT ⎍, EXT ⎏, (rotary selector switch)	CAL ⎍ (calibrated pulse) position internally pulse modulates the amplitude of RF OUT ⑭ signal at the 1 kHz rate, with a fixed 1 μs pulse width. The ⎍ (pulse) position internally pulse modulates the amplitude of RF OUT ⑭ signal. The ⎍⎍ (squarewave) position internally modulates the amplitude of RF OUT ⑭ signal with a 50% duty cycle. OFF position impresses no modulation on the RF OUT ⑭ signal. EXT ⎍ (leading edge) and EXT ⎏ (trailing edge) position allows an external squarewave or pulse on the MOD ② BNC connector to amplitude modulate the RF OUT ⑭ signal, triggered on the leading or trailing edge.
26	MOD P.R.F. 100 Hz - 10 kHz, 1 kHz PRESET (rotary control with detent)	1 kHz PRESET detent position on this control is used when the ⎍ or ⎍⎍ MODULATION ㉕ is selected and a calibrated 1 kHz pulse repetition frequency is desired. When rotated clockwise out of the detent position, the 100 Hz to 10 kHz pulse repetition frequency is selectable.
27	MOD P.R.F. X5 (pushbutton)	Pushbutton affects the MOD P.R.F. ㉖ 100 Hz to 10 kHz pulse repetition frequency control. Out position - multiplies the variable MOD P.R.F. ㉖ frequency range by 1, so that the range of this control is 100 Hz to 10 kHz (nominal). In position - multiplies the variable MOD P.R.F. ㉖ frequency range by 5, so that the range of this control is 500 Hz to 50 kHz (nominal).
28	PULSE WIDTH, μSEC, .1, 1, 10	Control is concentric with the MODULATION ㉕ switch and varies the pulse width of the ⎍ modulation pulse.

3-5. LOCAL OPERATING PROCEDURES

3-6. After installing Model 1626, as described in chapter 2, plug the synthesizer into an appropriate power source and energize the instrument by turning LINE ① switch to the ON position. The FREQUENCY, GHz ㉑ and POWER METER, dBm ⑱ displays will illuminate. Press the DISPLAY TEST ㉓ pushbutton to check that all display segments illuminate. Select a desired output frequency between 0.1 and 26 GHz by actuating the CW/START, GHz ㉒ leverwheel switch arms up or down. The signal on RF OUT ⑭ SMA connector will be the selected microwave frequency (after one-half hour warm-up). Also, proper sweep mode, leveling and attenuation, modulation, and reference source must be established for a valid output. Refer to the following procedures for proper adjustment of the output characteristics.

CAUTION

Damage may be sustained by the Model 1626 if greater than +20 dBm is impressed on the RF OUT ⑭ connector.

Damage may also be sustained by the power meter if greater than +20 dBm is applied to the EXT POWER METER INPUT ⑪.

NOTE

Model 1626 requires a warm-up period of approximately one-half hour after application of line power. The instrument is ready for operation when the LOCK ⑯ and LEVEL ⑰ lamps switch from red to green indication.

Table 3-2. Rear Panel, Model 1626

Index	Name	Function
1	Hex Nut	One of four mounting nuts that attach the air filter housing to the rear panel.
2	Air Filter Housing	Housing holds the air filter and is held on with four mounting nuts ①.
3	Air Filter	Metal air filter must be cleaned periodically. DO NOT OBSTRUCT AIR FLOW THROUGH THIS PORT.
4	PEN LIFT (BNC connector)	BNC connector provides a transistor switched-to-ground signal during sweep retrace.
5	REMOTE PROGRAMMING (24-pin connector)	Connector couples the instrument to GPIB IEEE Std 488-compatible equipment to permit remote programming of the unit.
6	REMOTE PROGRAMMING ADDRESS 1-5 (0-1 slide switches)	Five slide switches set the synthesizer address to a five-bit binary code in accordance with IEEE Std 488.
7	Air Exhaust (Fan)	Exhaust fan removes warm air from instrument cabinet. DO NOT OBSTRUCT AIR FLOW THROUGH THIS PORT.
8	AC Power Cord (Receptacle)	Receptacle accepts detachable six-foot power cord accessory.
9	Fuse Post (F1) Main Power 100/115 V ac operation 3 A 3AG SB 200/230 V ac operation 1.5 A 3AG SB	Holder retains the power fuse. To remove fuse, push in and turn cap in the direction of arrow. DISCONNECT SYNTHESIZER LINE CORD BEFORE REMOVING FUSE.
10	Transistors Q1/Q2	FET drivers for Q1 output and Q2 reference oscillators.

NOTE

An over-temperature protection feature is incorporated into Model 1626 which removes ac line power from the instrument whenever internal overheating occurs. If this happens, allow instrument to cool (approximately one-half hour to one hour): the instrument will automatically reset power at the end of this cooling period. During the shutdown period, check the temperature of rack cabinet air; look for external air-flow obstructions, dirty fan filter ③; and, when power is reapplied, be certain that the instrument fan ⑦ is operating properly.

3-7. Sweep Modes

3-8. One of three sweep modes may be selected for a proper swept signal. Sweep control utilizes four SWEEP ⑥ through ⑨ pushbuttons, the ΔF, GHz ⑳ leverwheel switches, and the SWEEP OUT ⑩ BNC connector. The cw mode does not provide for sweeping of the rf output. The .1 kHz ⑦ step rate mode permits sweeping up of the rf output frequency in 1 MHz steps at a 100 Hz rate from 0.010 to 9.999 GHz. The 1 kHz ⑥ step rate mode permits sweeping up of the rf output frequency in 1 MHz steps at a 1000 Hz rate over the same sweep range. The 1 step mode provides manual stepping of the CW/START, GHz ㉒ frequencies in 1 MHz increments to ΔF greater than 9.999 GHz. Reset mode manually sets the output frequency back to the CW/START, GHz ㉒ start frequency.

3-9. CW

3-10. Press CW ⑤ pushbutton. Set CW/START, GHz ㉒ leverwheel switch to the desired output frequency. RF OUT ⑭ SMA connector supplies the selected frequency when LOCK ⑯ and LEVEL ⑰ lamps are illuminated green. FREQUENCY, GHz ㉑ and POWER METER, dBm ⑱ display the frequency and power level at RF OUT ⑭ SMA connector.

3-11. .1 kHz Step Rate

3-12. Press .1 kHz (100 Hz) STEP RATE ⑦ pushbutton. Select a start frequency from 0.1 to 26 GHz with CW/START, GHz ㉒ leverwheel switches. Select a

sweep range from 0.010 to 9.999 GHz with ΔF, GHz ⑳ leverwheel switches. Be sure the sum of start frequency and sweep range is less than 26 GHz. The FREQUENCY, GHz ㉑ display will show the start frequency being counted up until it reaches the CW/START, GHz ㉒ + ΔF, GHz ⑳ frequency. At the end of the sweep, the display returns to the start frequency and repeats the up sweep. The 1 MHz steps occur at a 0.1 kHz rate or 1 MHz/10 ms. The SWEEP OUT ⑩ BNC connector provides a 0 to 10 V ramp with a period of ΔF × 10 ms for an external sweep sync.

3-13. 1 kHz Step Rate

3-14. Press 1 kHz (1000 Hz) STEP RATE ⑥ pushbutton. See paragraph 3-12 for operational procedures. In this sweep mode, however, the 1 MHz steps occur at a 1 kHz rate or 1 MHz/1 ms. The SWEEP OUT ⑩ BNC connector provides a 0 to 10 V ramp with a period of ΔF × 1 ms for an external sweep sync.

3-15. 1 Step

3-16. Select either the .1 or 1 kHz STEP RATE sweep mode, as described above. Pressing the 1 STEP ⑧ pushbutton will increment the rf output frequency by 1 MHz each time actuation takes place. The FREQUENCY, GHz ㉑ display shows the incremented output rf frequency.

3-17. Reset

3-18. In any of the sweep modes, pressing RESET ⑨ pushbutton will set the rf output back to the CW/START, GHz ㉒ leverwheel switch frequency.

3-19. Pen Lift

3-20. PEN LIFT ④ BNC connector on the rear panel of Model 1626 provides a transistor switched-to-ground signal during sweep retrace time.

3-21. Level and Attenuation

3-22. The rf output may be leveled at +5 dBm, or increased continuously to uncalibrated levels higher than +5 dBm in any of the sweep or modulation modes. A decade step attenuator ⑫, ⑬ provides 0 to −99 dB attenuation of the leveled output. The POWER METER, dBm ⑱ display continuously indicates the selected output level and may also be used to measure the power level of an external rf input.

3-23. Leveled

3-24. Rotate LEVEL ⑮ potentiometer counterclockwise to the LEVELED detent position. Set the −10 dB STEP ⑫ and −1 dB STEP ⑬ ATTENUATION switches to 0. Set the POWER METER ⑲ toggle switch to INT. The POWER METER, dBm ⑱ display will show an rf output level of +05.0 dBm. Various settings of the ATTENUATION switches ⑫, ⑬ will display calibrated +5 to −94 dBm levels on POWER METER, dBm ⑱.

3-25. Increase

3-26. Rotating LEVEL ⑮ potentiometer clockwise will uncalibrate the leveling control and increase the output above +5 dBm. After rotating the LEVEL control clockwise, set −10 dB STEP ⑫ and −1 dB STEP ⑬ ATTENUATION switches to 0. Set POWER METER ⑲ toggle switch to INT. The POWER METER, dBm ⑱ display will show an unleveled rf output from +5 dBm to typically +13 dBm; however, RF OUT ⑭ signal power will be essentially uncalibrated.

3-27. Attenuation

3-28. The rf output may be attenuated by these switches from 0 to −99 dB. Rotate −10 dB STEP ⑫ and −1 dB STEP ⑬ ATTENUATION switches so that the numerical sum equals the desired attenuation. When the LEVEL ⑮ switch is in LEVELED position, output power is 5 dB higher than the indicated attenuation setting. In the unleveled range of LEVEL ⑮ control, whatever power level is set, ATTENUATION ⑫, ⑬ switches will reduce that level by 0 to −99 dB. The POWER METER dBm display indicates the selected rf output power level.

3-29. External Power Meter

3-30. Set POWER METER ⑲ toggle switch to EXT. or EXT COMP. Connect the external 0.1 to 26 GHz rf source to the INPUT SMA ⑪ connector. Read power level in dBm on the POWER METER, dBm ⑱ display.

3.31 The range limits of external power measurement are +10 to −3 dbm, with an accuracyof ±1 dBm from +10 dBm to −10 dBm and ±2 dBm from −10 dBm to −30 dBm.

CAUTION

Damage to the power meter may be sustained if greater than +20 dBm is applied to the EXT POWER METER INPUT ⑪ connector.

3-32. Modulation

3-33. Model 1626 provides two types of internal amplitude modulation: pulse and squarewave. No modulation, as well as external amplitude modulation are also selectable. MOD ② BNC connector provides both output of the modulation signal and an input for the external modulation signal.

3-34. CAL ⎍ (Calibrated Pulse)

3-35. With the MODULATION ㉕ switch set to CAL ⎍, the rf output will be pulse modulated at a fixed 1 kHz rate. The pulse width will be a fixed 1 μs wide. The MOD ② BNC connector supplies a TTL-compatible output of the modulation pulse for external sync, etc.

3-36. ⎍⎍ (Pulse)

3-37. Set the MODULATION ㉕ switch to ⎍⎍ . Set the PULSE WIDTH ㉘ concentric control knob to the desired pulse width (.1 to 10 μs). The output will be 100% modulated at a 1 kHz rate and the rf burst out will have the same duration as the pulse width. The MOD ② BNC connector supplies a TTL-compatible output of the modulation pulse for external sync, etc. The rate is 1 kHz unless varied by the MOD P.R.F. ㉖, ㉗ controls.

3-38. ⎍⎍ (Squarewave)

3-39. Set the MODULATION ㉕ switch to ⎍⎍ . The output will be 30 dB am modulated at a 1 kHz rate and 50% duty cycle. The rf burst output will also have a 50% duty cycle with the rf turned on for the first half of the squarewave, and off (−30 dB) for the second half of the squarewave. The MOD ② BNC connector supplies a TTL-compatible modulation squarewave for external sync, etc. As previously mentioned, the MOD P.R.F. ㉖, ㉗ controls can vary the rate.

3-40. OFF

3-41. With MODULATION ㉕ switch set to OFF, output rf will have no modulation present.

3-42. EXT ⎍ (External Positive-Going Edge)

3-43. With MODULATION ㉕ switch set to EXT ⎍ , output rf may be externally pulse modulated with the external pulse signal coupled to the MOD ② BNC connector. The positive-going transition of the input pulse will trigger modulation: input should be a TTL-compatible signal.

3-44. EXT ⎍ (External Negative-Going Edge)

3-45. With MODULATION ㉕ switch set to EXT ⎍ , output rf may be externally pulse modulated with the external pulse signal coupled to the MOD ② BNC connector. In this case, the negative-going transition of the input pulse will trigger modulation: input should be a TTL-compatible signal.

3-46. MOD P.R.F. (Modulation Pulse Repetition Frequency)

3-47. Pulse repetition frequency may be varied from the standard 1 kHz preset value, if desired. The variable range is from 100 Hz to 10 kHz (nominal) when X5 ㉗ switch is deactivated, and 500 Hz to 50 kHz (nominal) when the switch is activated.

3-48. 1 kHz Preset

3-49. With MOD P.R.F. ㉖ control set in 1 kHz PRESET detent position, pulse repetition frequency will be a fixed 1 kHz.

3-50. 100 Hz - 10 kHz

3-51. With MOD P.R.F. ㉖ control in the variable position, the pulse repetition frequency may be set from 100 Hz to 10 kHz (nominal).

3-52. X5

3-53. With X5 ㉗ pushbutton in the activated position, the variable-pulse repetition frequency is multiplied by 5 to a range of 500 Hz to 50 kHz (nominal).

3-54. 1 MHz REF

3-55. The output rf is phase locked to either an internal 1 MHz reference or an external 1 MHz reference. The 1 MHz REF ③ BNC connector and ④ toggle switch are used with this feature.

3-56. Int

3-57. Select INT with 1 MHz REF ④ toggle switch. The synthesizer is now connected to the 1 MHz internal reference and 1 MHz REF EXT ③ BNC connector is providing reference signal as an output. Then, set the modulation, sweep, attenuation, and level modes, as required.

3-58. Ext

3-59. Select EXT with 1 MHz REF ④ toggle switch. Couple a 1 MHz, 2 V p-p reference signal to the 1 MHz REF EXT ③ BNC connector. The synthesizer is now locked to the external reference. Then, set the modulation, sweep, attenuation, and level modes, as required.

3-60. REMOTE OPERATING PROCEDURES (IEEE Std 488 GPIB)

3-61. Model 1626 may be remotely operated using the installed General Purpose Interface Bus (GPIB). This interface permits remote operation of the synthesizer from a data bus that conforms to IEEE Std 488-1978. See table 2-3, GPIB Interface Connector, data bus and control lines.

3-62. IEEE Std 488 Implemented Interface Function Subsets

3-63. Incorporated into Model 1626 are the interface function subsets listed in table 3-3 for implementation of IEEE Std 488-1978 GPIB.

3-64. GPIB Characteristics

3-65. For GPIB electrical and mechanical specifications see the referenced IEEE standard. The interface system contains a set of 16 signal lines to carry all information-interface messages and device-dependent messages. These messages may be coded on one, or a set of signal lines, determined by the particular message content.

NOTE

Model 1626 remote GPIB programming extends to all major front- and rear-panel controls, except ATTENUATION, −10 dB STEP ⑫, MOD P.R.F. ㉖, and PULSE WIDTH μSEC ㉘.

3-66. The bus structure consists of three sets of signal lines (see figure 3-3, for bus management information):

1. Data Bus - 8 signal lines.
2. Data Byte Transfer Control Bus - 3 signal lines.
3. General Interface Management Bus - 5 signal lines.

Table 3-3. Implemented Interface Function Subsets

Subset	Description	Capability
SH1	Source Handshake	Complete
AH1	Acceptor Handshake	Complete
T8	Talker	Basic Talker, (unaddress if MLA)
TE0	Extended Talker	None
L4	Listener	Basic Listener, (unaddress if MTA)
LE0	Extended Listener	None
SR0	Service Request	None
RL2	Remote Local	No Local Lockout
PP0	Parallel Poll	None
DC0	Device Clear	None
DT0	Device Trigger	None
C0	Controller	None

3-67. The mnemonics, DIO1 to DIO8, are assigned by IEEE Std 488 to eight data input/output lines. Message bytes are transferred on the DIO signal lines in a bit-parallel, byte-serial format, asynchronously, and usually bidirectionally. Mnemonic DIO8 is not used by Model 1626.

3-68. A set of three interface signal lines effect transfer of each byte of data on DIO signal lines, from an addressed talker to all addressed listeners:

1. DAV (data valid) indicates the condition (availability and validity) of information on DIO signal lines.
2. NRFD (not ready for data) indicates the readiness condition of device(s) to accept data.
3. NDAC (not data accepted) indicates the condition of acceptance of data by device(s).

3-69. The DAV, NRFD, and NDAC signal lines operate in what is called a three-wire (interlocked) handshake process to transfer each data byte across the interface.

3-70. Five interface signal lines are used to manage an orderly flow of information across the interface.

1. ATN (attention) specifies how data on DIO signal lines are to be interpreted and which devices must respond to the data.
2. IFC (interface clear) resets the interface system, portions of which are contained in all interconnected devices, into a known quiescent state.
3. SRQ (service request) is used by a device to indicate the need for attention and to request an interruption of the current sequence of events. This line is not used in Model 1626.
4. REN (remote enable) is used (in conjunction with other messages) to select between two alternate sources of device programming data.
5. EOI (end or identify) indicates the end of a multiple-byte transfer sequence or, in conjunction with ATN, the execution of a polling sequence. This line is not used in Model 1626.

3-71. Address Assignment Procedure

3-72. The rear-panel, 5-digit ADDRESS switches are used to set talk and listen addresses used by the synthesizer. Thirty-one talk addresses and thirty-one listen addresses may be assigned. See table 3-4 for address switch settings, and corresponding listen and talk ASCII characters.

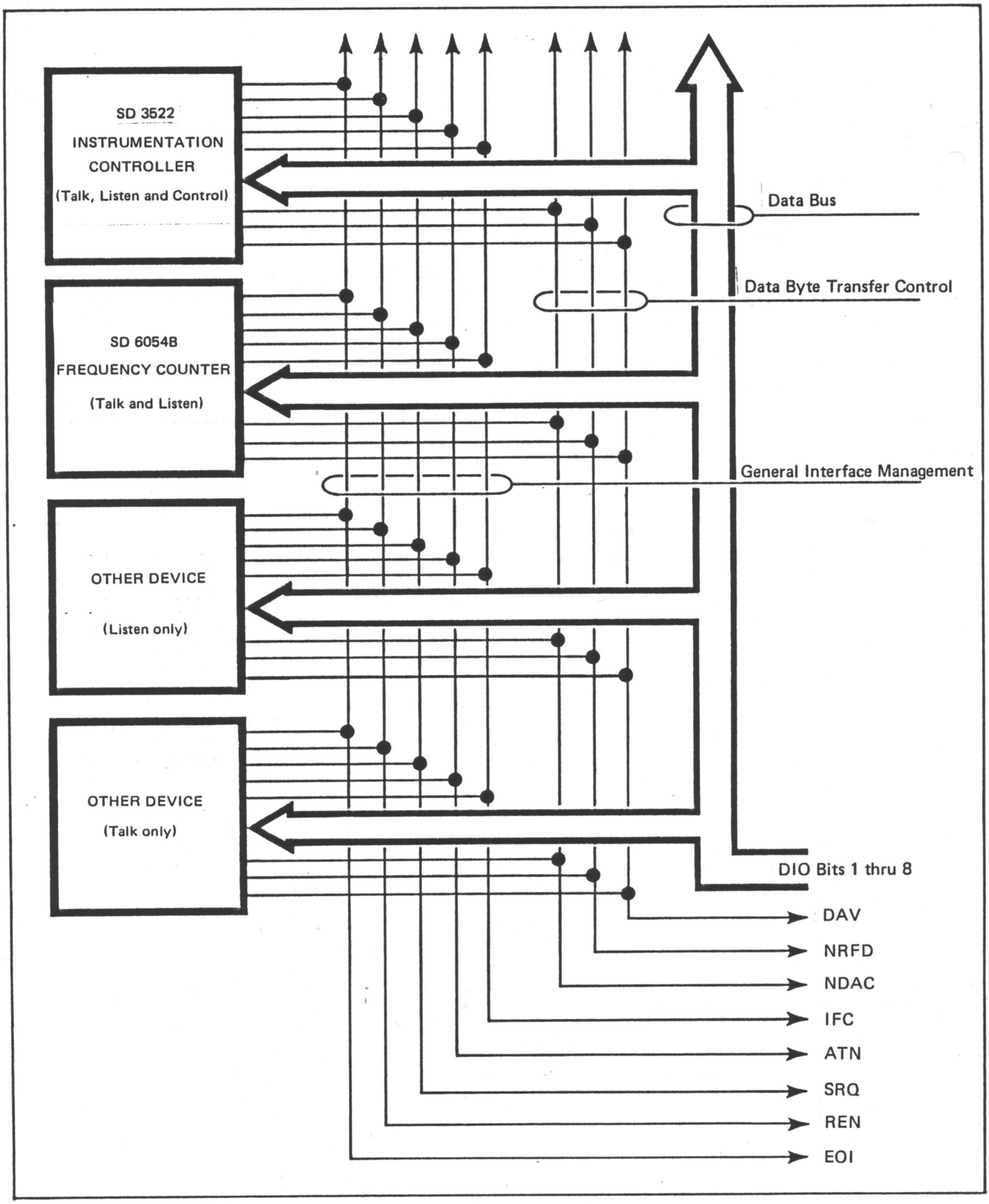


Figure 3-3. GPIB Interface Capabilities and Bus Structure

Table 3-4. Talk/Listen Address vs. ASCII Character

Address Switch Settings					ASCII Character	
5	4	3	2	1	Listen	Talk
0	0	0	0	0	SP	@
0	0	0	0	1	!	A
0	0	0	1	0	"	B
0	0	0	1	1	#	C
0	0	1	0	0	$	D
0	0	1	0	1	%	E
0	0	1	1	0	&	F
0	0	1	1	1	'	G
0	1	0	0	0	(	H
0	1	0	0	1	)	I
0	1	0	1	0	*	J
0	1	0	1	1	+	K
0	1	1	0	0	,	L
0	1	1	0	1	−	M
0	1	1	1	0	.	N
0	1	1	1	1	/	O
1	0	0	0	0	0	P
1	0	0	0	1	1	Q
1	0	0	1	0	2	R
1	0	0	1	1	3	S
1	0	1	0	0	4	T
1	0	1	0	1	5	U
1	0	1	1	0	6	V
1	0	1	1	1	7	W
1	1	0	0	0	8	X
1	1	0	0	1	9	Y
1	1	0	1	0	:	Z
1	1	0	1	1	;	[
1	1	1	0	0	<	\
1	1	1	0	1	=	]
1	1	1	1	0	>	^
1*	1	1	1	1	?	−

*Not to be device assigned. Refer to note.

NOTE

A 11111 address must not be assigned to any unit interfacing the bus since this listen and talk address is reserved for the UNL (unlisten) ASCII (?) and the UNT (untalk) ASCII (−) command.

3-73. To address Model 1626 talk or listen capability, set rear-panel REMOTE PROGRAMMING switches, 1 through 5, to a valid talk or listen address. Couple IEEE Std 488 24-pin cable to the rear-panel REMOTE PROGRAMMING connector. Program the controller to set ATN line to 1, and send UNL command to inhibit all current listeners. Now, send the listen or talk address of Model 1626. When ATN goes to 0, the synthesizer will listen or talk. To enter a program, set the ATN line to 1 again, and send program data.

3-74. Frequency Data Entry Procedure

3-75. With the synthesizer addressed to listen, an ASCII letter followed by an ASCII number, will be treated as a CW/START, GHz ㉒ frequency digit (address character) followed by the numerical value (digital character) of the digit. Table 3-5 lists valid address and digital characters for the remote CW/START, GHz ㉒ frequency.

3-76. An example of the program required to select CW/START, GHz ㉒ frequency 12.345 GHz is H1G2F3E4D5. Also, the order of each numerical value with its alphabetic address may be randomly entered, such as H1G2F3D5E4.

Table 3-5. CW/START, GHz Frequency Program Coding

ASCII Code	Internal Function
H	Selects 10 GHz Digit
0-2	Value of 10 GHz Digit
G	Selects 1 GHz Digit
0-9	Value of 1 GHz Digit
F	Selects 100 MHz Digit
0-9	Value of 100 MHz Digit
E	Selects 10 MHz Digit*
0-9	Value of 10 MHz Digit*
D	Selects 1 MHz Digit*
0-9	Value of 1 MHz Digit*

*Valid selections outside limits imposed by table 1-1, Specifications.

3-77. Digit characters in a frequency program string which are not preceded by an alphabetic address character, will decrement one position from the last alphabetic address for each digit character entered; thus, automatically selecting the next most significant digit. Because of this, frequency 12.345 GHz may also be selected with H12345, or F3H1G2E45.

3-78. To change frequency by small increments after frequency is programmed, it is only necessary to enter ASCII alphabetic address and digit value desired. For example, to change the previously programmed 12.345 GHz frequency to 12.346 GHz, just enter a program string of D6.

3-79. Model 1626 synthesizer ignores ASCII characters . , / ! + − in a program string, as well as those characters not included in its programming code. A data zero will be entered for blanks in the string.

3-80. Preceding the ASCII alphabetic address with ASCII letter W allows new data to be shifted into the internal register. But data from the register will not be shifted to the synthesizer until an ASCII letter T, line feed (LF), or a carriage return (CR) is entered.

3-81. Sweep Data Entry Procedure

3-82. With the synthesizer addressed to listen, designated ASCII letters, followed by an ASCII number, will be treated as a ΔF, GHz ⑳ sweep frequency digit (address character) followed by a numerical value (digital character) for the digit. Table 3-6 lists the valid address and digital characters for the remote ΔF, GHz ⑳ sweep frequency. Sweep data programming is identical to the programming described in paragraphs 3-75 through 3-80 for frequency selection.

Table 3-6. ΔF, GHz Frequency Program Coding

ASCII Code	Internal Function
C	Selects 1 GHz digit
0-9	Value of 1 GHz digit
B	Selects 100 MHz digit
0-9	Value of 100 MHz digit
A	Selects 10 MHz digit
0-9	Value of 10 MHz digit
@	Selects 1 MHz digit*
0-9	Value of 1 MHz digit*

*Valid selections outside limits imposed by table 1-1, Specifications.

3-83. Sweep Function Entry Procedure

3-84. The sweep function is selected using ASCII alphanumeric codes O,0 through O,8. A list of these codes and functions will be found in table 3-7. CW, or no sweep, is selected with an ASCII O,1 entry. The 1 kHz (1 ms/step) and 0.1 kHz (10 ms/step) sweeps are selected with an ASCII O,2 and O,3 entry, respectively. ΔF, GHz ⑳ frequency selections may be incremented in 1 MHz steps by selecting O,4. Selecting O,8 code will reset the RF OUT ⑭ back to CW/START, GHz ㉒ frequency. The single-step mode permits the operator to select a sweep speed other than fixed 100 Hz or 1 kHz, and a ΔF larger than 9.999 GHz.

Table 3-7. Sweep Function Program Coding

ASCII Code*	Internal Function
O,1	Selects CW (no sweep)
O,2	Selects 1 kHz STEP RATE SWEEP (1 ms/STEP)
O,3	Selects 0.1 kHz STEP RATE SWEEP (10 ms/STEP)
O,4	Selects 1 STEP SWEEP (single step).
O,8	Selects RESET SWEEP.

*NOTE: Alphabetic O, numeric 1, 2, 3, 4, and 8.

3-85. Attenuation Data Entry Procedure

3-86. The −1 dB STEP ⑬ attenuator may be remotely adjusted using ASCII L0 to L9, representing 0 to −9 dB in one dB attenuation steps. The LEVEL ⑮ vernier control is set from 0 to +9 dB in one dB steps using ASCII M0 to M9. The −10 dB STEP attenuator may only be set manually. See table 3-8, listing ASCII codes for remote attenuation data entry.

Table 3-8. Attenuation and Vernier Program Coding

ASCII Code	Internal Function
L0	−0 dB step attenuation
L1	−1 dB step attenuation
L2	−2 dB step attenuation
L3	−3 dB step attenuation
L4	−4 dB step attenuation
L5	−5 dB step attenuation
L6	−6 dB step attenuation
L7	−7 dB step attenuation
L8	−8 dB step attenuation
L9	−9 dB step attenuation
M0	+5 dBm level
M1	+6 dBm level
M2	+7 dBm level
M3	+8 dBm level
M4	+9 dBm level
M5	+10 dBm level
M6	+11 dBm level
M7	+12 dBm level
M8	+13 dBm level
M9	+14 dBm level

NOTE: Overranging of LEVEL control may exceed the output capability of synthesizer on upper M ranges.

3-87. Modulation Function Entry Procedure

3-88. Modulation functions are remotely selected using ASCII N0 to N4 codes. Table 3-9 lists each code and its function. OFF, or no modulation is selected with ASCII code N0. CAL ⎍⎍ , or a calibrated fixed 1 kHz pulse, 1 μs wide, is selected with the ASCII code N1. 1 kHz squarewave ⎍⎍⎍ modulation is selected with an ASCII N2. The ASCII N3 is used to select EXT ⎍ pulse modulation with a positive-going edge trigger. N4 selects EXT ⎾⎍ pulse modulation with a negative-going edge trigger.

Table 3-9. Modulation Program Coding

ASCII Code	Internal Function
N0	Selects OFF (no modulation)
N1	Selects CAL ⎍⎍ (calibrated pulse)
N2	Selects ⎍⎍⎍ (squarewave)
N3	Selects EXT ⎍ (external, positive-going edge trigger)
N4	Selects EXT ⎾⎍ (external, negative-going edge trigger)

3-89. Status Reporting - Talk Mode

3-90. The operating status of Model 1626 is sent when the instrument is addressed to talk after data is received. Operating status is outputted in octal form, followed by a carriage return (CR) and a line feed (LF). Table 3-10 lists the ASCII codes for the indicated status.

Table 3-10. Status Output Coding

ASCII Code Output	Internal Status
0, CR, LF	Locked and Leveled
1, CR, LF	Unlocked and Leveled
2, CR, LF	Locked and Unleveled
3, CR, LF	Unlocked and Unleveled

CHAPTER 4

THEORY OF OPERATION

4-1. INTRODUCTION

4-2. Model 1626 Microwave Synthesizer has been designed to generate signals in the 0.1 to 26 GHz range. The output frequency is derived from, and phase locked to, a stable TCXO source, thereby translating the source stability of 1 ppm/year to the output. Use of Yttrium-Iron-Garnet (YIG) devices as reference oscillators, output oscillators, and a tunable band-pass filter provides spectral purity of a very high order (all harmonic and spurious signals are less than −55 dBc). Output frequency may be incremented in 1 MHz steps from 10 MHz to 9.999 GHz, under instrument control while in a repetitive mode, thus providing a sweep function. The output level is controlled by a closed-loop leveling system and step attenuators, providing an accuracy of ±1 dB to 18 GHz and ±2 dB above 18 GHz. Pulse modulation may also be applied to the output, with peak power remaining under leveling control. The synthesizer can be operated remotely via IEEE Std 488 (GPIB), providing control of all operational parameters, except on/off power, power meter functions, modulation PRF, and pulse width.

4-3. The Model 1626 theory of operation is presented from three perspectives: The frequency synthesis/leveling techniques are discussed first, and are referenced to figure 4-1, Signal Generation. Second, an overview of functional operation at the block diagram level is provided and referenced to figures 7-1, 7-2, 7-3, located in chapter 7. Third, a detailed description of circuitry contained on the functional assemblies is presented and referenced to schematic diagrams in chapter 7.

4-4. FREQUENCY SYNTHESIS AND LEVELING

4-5. The frequency synthesis technique requires three separate functional phase-lock loops, which are defined as follows:

1. Reference loop; phase locks a YIG reference microwave oscillator to a specific comb line.
2. Divide-by-N loop; generates the one and ten MHz steps of the synthesis function.
3. Output loop; completes the synthesis functions by combining the coarse steps of the reference loop and the five steps of the divide-by-ten loop.

4-6. Reference Loop

4-7. The reference loop provides for locking of the selected reference YIG oscillator to a 100 MHz comb line. In order to reduce the frequency range required of the reference YIG oscillator, the fundamental frequency is used for output frequencies between 2.0 and 5.9 GHz. Below 2.0 and above 5.9 GHz, the third harmonic of the reference oscillator is used (which is generated by sampler/mixer,U14). This scheme requires only a reference oscillator range of 1.9 to 8.7 GHz. Two different YIG oscillators are actually used to cover this range: one is the 1.9 to 6 GHz YIG oscillator, Y1; the other is the 4 to 8.7 GHz YIG oscillator, Y2, which also functions as the down-converter loop oscillator.

4-8. The reference oscillator frequency is first coarse tuned by stepping the oscillator to a point that is close to the desired output. This is accomplished with the A6 D/A converter which converts the digital tens and ones GHz data to a coarse-tuned drive. This drive is applied to the selected reference YIG via FET driver, Q2, and FET switching circuits located in assembly A26. The output from the reference oscillator is coupled by U13 to sampler/mixer, U14, which is driven by the 33.33 MHz reference signal. Whenever the reference oscillator output is sufficiently close to a multiple of 33.33 MHz, U14 will generate an intermediate frequency (i f). This i f signal is then applied to the reference phase detector, located on assembly A14, which outputs to the reference oscillator as a fine-tune signal to complete the tuning process. This allows the reference oscillator to lock up every 33.33 MHz. Below 6 GHz, fundamental mixing is used: the coarse tuning step is provided to lock on every 100 MHz (3 comb lines). Above 6 GHz the sampler mixer, U14, triples the oscillator output frequency so that the oscillator not only runs at a third of the "desired" output frequency, but also increments by a third of 100 MHz (33.33 MHz).

4-9. Output Loop

4-10. To generate the synthesized output frequency, one of five YIG output oscillators (Y2 through Y6) is selected by FET switching circuitry located on assembly A26. YIG output oscillator selection is based on the frequency control data. The selected YIG oscillator is then coarse tuned by the D/A converter, located on assembly A6, in the same manner as the reference oscillator described in paragraph 4-7. A sample of the output YIG oscillator is coupled by the appropriate leveling module (U5, U8, or U11) to mixer, U16, which has the reference oscillator as its other input. Mixer, U16, outputs a frequency of 99 to 198 MHz, which is divided by ten and applied to the output phase-lock loop phase detector. Both the divide-by-ten counter and phase detector are located on assembly A13.

4-11. Divide-by-N Loop

4-12. The output phase-lock loop (assembly A13) compares mixer, U16, output with output from the divide-by-N assembly, A10. The divide-by-N phase-lock loop generates a 9.9 to 19.8 MHz output in steps of 1 and 0.1 MHz. Since the phase detector, located on assembly A13, sees a variable input, it will "force" the controlled element of the output phase-lock loop (output YIG oscillator) to follow. It should be noted that a times ten resolution is provided by the divide-by-ten counters located on assemblies A10 and A13, thus effectively locking up the synthesis to 1 MHz steps.

4-13. 33.33 MHz Reference

4-14. Assembly A12 provides frequency outputs of 33.33, 10, 1, and 0.1 MHz, which are derived via a phase-lock loop and down counters, from the 10 MHz VCO located on assembly A18. This 10 MHz VCO, in turn, is phase-locked to the TCXO internal source, thereby translating its base 1 ppm/year stability to the synthesized output. An external 1 MHz frequency standard may be applied and switch selected (via the front panel) when greater stability is required.

4-15. Down Conversion

4-16. When the synthesizer is outputting a 0.1 to 1.999 GHz signal, down conversion is provided by mixer, U17. A sample of the selected output YIG oscillator, Y4, is coupled via 2 to 12 GHz leveling module, U5, to mixer, U17. The other input to mixer, U17, is derived from the down converter phase-lock loop comprised of YIG oscillator, Y2; 4-8 GHz coupler, U1; sampler, U15; fixed LO assembly, A11; and sampler driver assembly, A20. Mixer, U17, outputs an 8 to 10 GHz signal to the down converter, comprised of assembly A21; 0.5 to 2 GHz amplifier, U18; and low-pass filters, FL3 through FL6.

4-17. Leveling

4-18. Synthesizer output power is controlled by a feedback, closed-loop system, plus two step attenuators. Two feedback subsystems are used to level the full frequency range of the synthesizer. One subsystem covers the 0.1 to 0.999 GHz range, while the other covers the 1 to 26 GHz range. The 0.1 to 0.999 GHz level is sampled and detected by U19 and U20; the 1 to 26 GHz level by U21 and U22. Detected level is switch selected and applied to a logarithmic amplifier by video amplifier assembly, A22. The logarithmic amplifier circuitry converts the square-law detector output into a lin-log signal that is relative to a dB level. The video amplifier output is applied to level control assembly, A3, where it is compared to the combination of selected output settings and correction factors. The comparator then drives the leveling PIN diode attenuators, located in leveling modules U5, U8, and U11, to maintain the correct output level.

4-19. To maintain the specified output level accuracy, it is necessary to compensate for coupler, detector, and step attenuator errors. This error correction data is computer processed and stored in programmable read only memory (2 PROMs), located on level control assembly, A3. As the frequency and/or step attenuator settings are changed, the correction circuitry reads the stored data and performs the required compensation, thus maintaining the specified leveling accuracy.

4-20. Modulation

4-21. Modulation of the output is provided as square-wave (0.5 duty cycle), or pulse. Variable, or fixed rate (prf) is front panel selectable, as is variable, or fixed duration (width), when pulse mode is selected. The modulation is accomplished by modulation PIN diode switches located in leveling modules U5, U8, and U11. Level control, when in the modulation pulse mode, is provided by pulse sampling circuitry. When modulation is selected, the pulse sampling circuitry is inserted into the leveling loop, thus providing leveling, as described in paragraph 4-18.

4-22. Harmonic Suppression

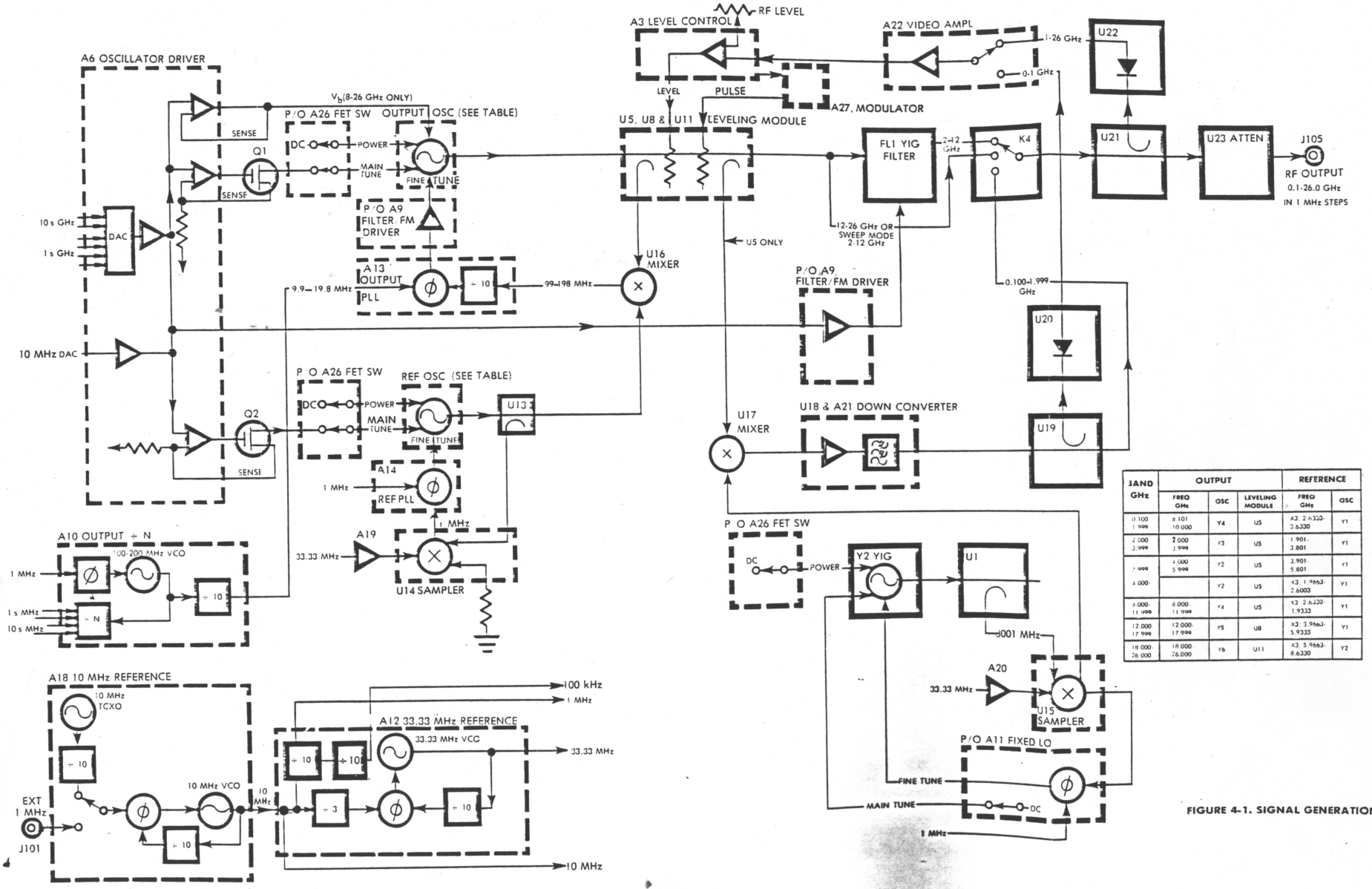
4-23. Harmonic suppression over the 2 to 12 GHz band is provided by YIG filter, FL1. When the synthesizer is operating in the 0 to 2 or 12 to 26 GHz band, the YIG filter is bypassed by the switching of relay, K4. Relay, K4, also provides selection of the 0.1 to 1.999 GHz down conversion, as described in paragraph 4-16. When down conversion is selected, harmonic suppression is provided by harmonic filters located on assembly A21, and/or low-pass filters, FL3 through FL6.

4-24. OVERALL FUNCTIONAL OPERATION

4-25. The following paragraphs (4-26 through 4-102) provide an overview of the Model 1626 functional operation. This discussion is referenced to three functional diagrams located in chapter 7 (figures 7-1, 7-2 and 7-3).

4-26. Six different configurations of the microwave devices contained in the synthesizer are selected by radio frequency (rf) relays. These different configurations relate to six frequency bands. Table 4-1 provides a tabulation by frequency band of the devices and their function as related to the reference and output phase-lock loops (PLLs).

4-27. When the synthesizer is operating in the 0.1 to 2 GHz band, another PLL is configured into the system to provide down conversion. YIG oscillator Y2 is switch selected as the down converter oscillator and tuned to 8.001 GHz.



JAND GHz	OUTPUT			REFERENCE	
	FREQ GHz	OSC	LEVELING MODULE	FREQ GHz	OSC
0.100 1.999	8.101 10.000	Y4	U5	X3: 2.7033- 3.3333	Y1
2.000 3.999	2.000 3.999	Y3	U5	1.901- 3.801	Y1
4.000 5.999	4.000 5.999	Y2	U5	3.901 5.801	Y1
6.000-		Y2	U5	X3: 1.9663- 2.6003	Y1
8.000- 11.999	8.000- 11.999	Y4	U5	X3: 2.6220- 3.9333	Y1
12.000 17.999	12.000- 17.999	Y5	U8	X3: 3.9663- 5.9333	Y1
18.000 26.000	18.000 26.000	Y6	U11	X3: 5.9663- 8.6330	Y2

FIGURE 4-1. SIGNAL GENERATION

Table 4-1. Frequency Band RF Device Relationship

Band GHz	Reference PLL		Output PLL		
	Osc.	Frequency GHz	Osc.	Leveling Module	Frequency GHz
0.1-2	Y1	(X3)2.6330—3.6330	Y4	U1 and U5	8.101—10.000
2-4	Y1	1.901—3.801	Y3	U5	2.000—3.999
	Y1	3.901—5.801	Y2	U5	4.000—5.999
4-8	Y1	(X3)1.9633—2.6003	Y2	U5	6.000—7.999
8-12	Y1	(X3)2.6330—3.9333	Y4	U5	8.000—11.999
12-18	Y1	(X3)3.9663—5.9333	Y5	U8	12.000—17.999
18-26	Y2	(X3)5.9663—8.6330	Y6	U11	18.000—26.500

4-28. 0.1 TO 2 GHz BAND FUNCTIONAL OPERATION

4-29. 0.1 to 2 GHz Reference PLL

4-30. YIG reference oscillator Y1 outputs a 2.6330 to 3.6330 GHz signal via semi-rigid coax cable W12 to transfer switch relay K1. Relay K1 switches the reference oscillator output via semi-rigid coax cable W10 to 2 to 8 GHz coupler U13. A sample of the reference oscillator signal is coupled by U13 to sampler U14 via semi-rigid coax cable W9. The 33.33 MHz reference signal from assembly A12 pin C is applied to sampler U14 via cable W46, sampler/driver A19 and cable W47. Sampler U14 outputs to the reference PLL assembly A14.

4-31. PLL assembly A14 provides the phase detection for the reference loop. Sampler U14 output is phase detected with a 0.333 MHz reference to generate a tuning signal (FM−) at A14 pin C. This FM− signal is applied to YIG reference oscillator Y1, thus closing the reference PLL. The output of 2 to 8 GHz coupler U13 is fed directly to 2 to 26 GHz mixer U16 via a SMA male-to-male connector to apply reference to the output PLL.

4-32. 0.1 to 2 GHz Band Output PLL

4-33. Output YIG oscillator Y4 supplies 8.101 to 10.000 GHz signal via a SMA male-to-male connector to isolator U4. Isolator U4 output is coupled to relay K2 via an attenuator pad and semi-rigid coax cable W2. Relay K2 switches the output YIG oscillator signal to U5 2 to 12 GHz leveling module via semi-rigid coax cable W17 and an attenuator pad. A sample of the output oscillator signal is coupled-off U5 via semi-rigid coax cable W18 to relay K3. Relay K3 switches the oscillator sample to the 2 to 26 GHz mixer U16 via semi-rigid coax cable W32. U16 mixes the oscillator sample with the reference oscillator output from the 2 to 8 GHz coupler U13, and outputs a 99 to 198 MHz intermediate frequency (i f) to A13 output PLL assembly via coax cable W41.

4-34. Assembly A13 provides the phase detection for the output PLL. The 99 to 198 MHz i f signal is referenced with the 10 to 19.9 MHz ÷10 signal from the ÷10 assembly A10 to generate the FM DRIVE signal, that outputs at A13 pin Y, to the YIG filter/FM driver assembly A9.

4-35. Assembly A9 provides the fine tuning drive at pin 10 to the output YIG oscillator Y4, thus closing the output PLL. Main tune drive for YIG oscillator Y4 is provided by the 8-12 V_b signal from oscillator driver assembly A6 pin E.

4-36. 0.1 to 2 GHz Down Converter PLL

4-37. YIG down converter oscillator Y2 outputs via a SMA male-to-male connector to the 4 to 8 GHz coupler U1. The down converter oscillator signal is coupled off U1 and applied via semi-rigid coax cable W13 to sampler U15. A 33.33 MHz reference signal from assembly A12 pin B is applied to sampler U15 via semi-rigid coax cable W44, sampler driver A20 and semi-rigid coax cable W48. U15 outputs to the fixed LO assembly A11 via cable W42.

4-38. Assembly A11 provides the phase detection for the down converter PLL. The i f signal from sampler U15 is referenced to a 1 MHz signal to generate a phase detection tuning signal at A11 pin M (FM−). The FM− signal is applied to down converter oscillator Y2, thus closing the down converter PLL.

4-39. Sampler U15 other output is directly coupled via a male-to-male SMA connector to the 8 to 12 GHz mixer U17. The other input to mixer U17, is the Y4 output oscillator derived signal, which is coupled off the 2-12 GHz leveler module U5 and applied via semi-rigid coax cable W14 and an attenuator pad.

4-40. Down Converter and Harmonic Filter Circuit

4-41. The output of mixer U17 is applied via semi-rigid coax cable W22 to the down converter and harmonic filter assembly A21 at its input connector J1. Assembly A21 provides switching selection of the filter configuration, which allows for different cutoff frequencies to be inserted into the signal path. Digital

frequency selection data from the frequency control assembly A7 is decoded by a PROM, and then processed to provide relay drive selection to relays K5 and K6.

4-42. When a frequency that is greater than 0.5 GHz is selected, the down converted signal at A21J2 is applied to the 0.5 to 2 GHz amplifier U18 via an attenuator pad and semi-rigid coax cable W23. Amplifier module U18 outputs via semi-rigid coax cable W25 to relay K5. The selection of low pass filter FL3, FL4 or FL5 is provided by relays K5 and K6 depending on the frequency selection relay drive signal at A21 pins 19, 20 or 21.

4-43. When a frequency less than 0.5 GHz is selected, the down converted signal is passed through a 50 to 500 MHz amplifier and one-of-four harmonic filters located within the A21 assembly. This signal is then applied to the 500 MHz low pass filter FL6 via semi-rigid coax cable W20. Filter FL6 outputs to relay K6J4 and is selected as the down converter 0.05 to 0.5 GHz signal by relay drive signal at A21 pin 12.

4-44. 0.1 to 2 GHz Output Leveling Circuits

4-45. The selected down converted output is routed from relay K6 to the front panel RF OUT connector J105; via 0.1 to 2 GHz coupler U19 relay K4, 1 to 26 GHz coupler U21 and step attenuator module U23, by semi-rigid coax cables W29, W7 and W8 respectively.

4-46. A sample of the output signal is coupled off the 0.1-1 GHz coupler U19, detected by U20 and applied to video amplifier A22 connector J1 via semi-rigid coax cable W57. Another sample is also coupled off 1-26 GHz coupler U21, detected by U22 and applied to A22 at connector J2.

4-47. Two A22 logarithmic amplifier circuits convert the square-law detector outputs into lin-log signals. A relay controlled by the 0 to 1 GHz switch, drives signal from the level control assembly A3 pin E, selects one of the amplifier outputs and applies it to A22J3 (detector out).

4-48. The level control assembly A3 receives the detector out signal from A22J3 via coax cable W56, and generates the 2 to 12 GHz level signal. This leveling signal outputs at A3 pin 6 and is applied via coax cable W51 to the 2 to 12 GHz leveling module U5. The leveling signal biases a PIN diode to attenuate the output of U5, thus maintaining a +5 dBm ±1 dBm leveled output into the step attenuator U23.

4-49. 2 TO 4 GHz BAND FUNCTIONAL OPERATION

4-50. 2 to 4 GHz Reference PLL

4-51. YIG reference oscillator Y1 outputs a 1.901 to 3.801 GHz signal via semi-rigid coax cable W12 to transfer switch relay K1. Relay K1 switches the reference oscillator output via semi-rigid coax cable W10 to 2 to 8 GHz coupler U13. Remainder of the reference PLL operation is similar to the 0.1 to 2 GHz reference PLL as described in paragraphs 4-30 and 4-31.

4-52. 2 to 4 GHz Band Output PLL

4-53. Output YIG oscillator Y3 supplies a 2.000 to 3.999 GHz signal via semi-rigid coax cable W39, isolator U3, an attenuator pad and semi-rigid coax cable W16 to switching relay K2. Relay K2 switches the output YIG oscillator signal to U5 the 2 to 12 GHz leveling module via semi-rigid coax cable W17 and an attenuator pad. The remainder of the output PLL operation is similar to the 0.1 to 2 GHz output PLL as described in paragraphs 4-33 and 4-34.

4-54. Assembly A9 provides the fine tuning drive at pin 9 to the output YIG oscillator Y3, thus closing the output PLL. Main tune drive for YIG oscillator Y3 is provided by the Y3-T signal from oscillator FET switch assembly A26 pin 9.

4-55. 2 to 4 GHz Output Leveling Circuits

4-56. The 2.000 to 3.999 GHz signal output of the 2 to 12 GHz leveler module U5 is applied to transfer switch relay K7 via semi-rigid W33. Relay K7 routes the output signal directly to relay K4 via semi-rigid coax cable W37 when the CW mode is selected.

4-57. When the sweep mode (ΔF) is selected relay K4 inserts YIG filter FL1 into the output signal path via semi-rigid coax cables W6 and W35. The YIG band pass filter FL1 is tuned by the YIG filter drive via a shielded pair from assembly A9 pins D (T−), R (+5 V) and A (Gnd). When the synthesizer is operating in the 0.1 to 2 GHz band, the filter provides harmonic suppression over the 2 to 12 GHz band. The YIG filter is then switched out of the output signal path.

4-58. Relay K4 selects the 2.000 to 3.999 GHz output signal and routes it to the 1 to 26 GHz coupler U21 via semi-coax cable W8. Output of U21 is directly coupled via an SMA male-to-female connector to step attenuator A23. The step attenuator then outputs to the front panel RF OUT SMA connector J105.

4-59. A sample of the output signal is coupled off U21, detected by U22 and applied to A22 at connector J2. A logarithmic amplifier circuit contained in A22 converts the square-law detector output of U21, into a lin-log signal, and outputs it at A22J3 (detector out).

4-60. The level control assembly A3 receives the detector out signal from A22J3 via semi-rigid coax cable W56 and generates the 2 to 12 GHz level signal. This leveling signal outputs at A3 pin 6 and is applied via coax cable W51 to the 2 to 12 GHz leveling module U5. The leveling signal biases a PIN diode to attenuate the output of U5, thus maintaining a +5 dBm ±1 dBm leveled output into the step attenuator U23.

4-61. 4 TO 8 GHz BAND FUNCTIONAL OPERATION

4-62. 4 to 8 GHz Reference PLL

4-63. YIG reference oscillator Y1 outputs a 3.901 to 5.801 GHz (X1) signal when the synthesizer is operating in the 4.000 to 5.999 range and 1.9633 to 2.6003 GHz (X3) when operating in the 6.000 to 7.999 GHz range. Operation of the reference PLL is similar to the 0.1 to 2 GHz reference PLL described in paragraphs 4.30 and 4.31.

4-64. 4 to 8 GHz Band Output PLL

4-65. Output YIG oscillator Y2 supplies a 4.000 to 7.999 GHz signal to the 4 to 8 GHz coupler U1 via a male-to-male SMA connector. Coupler U1 outputs to transfer switch K1 via isolator U2 and semi-rigid coax cable W11. Transfer switch K1 routes the output YIG signal to relay K2 via semi-rigid coax cable W15 and an attenuator pad. Relay K2 selects and applies the signal to the 2 to 12 GHz leveler module U5.

4-66. Two different PLL configurations are used for the 4 to 8 GHz band. When outputting in the 4.000 to 5.999 GHz range, a reference oscillator signal of 3.901 to 5.801 GHz is mixed utilizing sampler U15. When outputting in the 6.000 to 7.999 GHz range, a reference oscillator signal of 1.9663 to 2.6003 GHz is mixed utilizing mixer U16.

4-67. A sample of the 6.000 to 7.999 GHz signal is coupled off leveler module U5 and applied to relay K3 via semi-rigid coax cable W18. Relay K3 switches the signal to mixer U16 via semi-rigid coax cable W32. The 1.9663 to 2.6003 GHz Y1 reference oscillator signal is applied to the other input of mixer U16 via semi-rigid coax cable W12, transfer switch K1, coupler U13 and a male-to-male SMA connector.

4-68. Mixer U16 outputs a 99 to 198 MHz i f signal to the output PLL assembly A13 SMB connector J1 via coax cable W41. Assembly A13 provides the phase detection for the output PLL. The 99 to 198 MHz i f signal is referenced with the 10 to 19.9 MHz ÷ 10 signal from the ÷ 10 assembly A10 to generate the FM DRIVE signal that outputs at A13 pin Y. This FM DRIVE signal is applied to A9 YIG filter/driver assembly which outputs the FM− drive at its pin 8 to YIG Y2, thus closing the 6.000 to 7.999 GHz loop.

4-69. A sample of the 4.000 to 5.999 GHz is coupled off 4 to 8 GHz coupler U1 and applied via semi-rigid coax cable W13 to sampler U15. The 4.000 to 5.999 GHz output YIG sample is mixed with a 33.33 MHz reference signal from sampler driver A20, which is applied via semi-rigid coax cable W43. Sample U15 outputs the resultant as an i f signal via coax cable W42 to the fixed LO assembly A11.

4-70. Assembly A11 provides the phase detection for the PLL. The i f signal from sampler U15 is referenced to a 1 MHz signal to generate a tuning drive at A11 pin M (FM−). This FM− signal is applied to oscillator Y2 thus closing the 4.000 to 5.999 GHz output PLL.

4-71. 4 to 8 GHz Output Leveling Circuits

4-72. The 4 to 7.999 GHz output and leveling configuration is identical to the 2 to 4 GHz circuits described in paragraphs 4-55 through 4-60.

4-73. 8 TO 12 GHz BAND FUNCTIONAL OPERATION

4-74. 8 to 12 GHz Reference PLL.

4-75. YIG oscillator Y1 outputs a 2.6330 to 3.9333 GHz (X3) signal. Operation of the reference PLL is similar to the 0.1 to 2 GHz reference PLL described in paragraphs 4-30 and 4-31.

4-76. 8 to 12 GHz Band Output PLL

4-77. Output YIG oscillator Y4 provides an 8.000 to 11.999 GHz signal to relay K2 via isolator U4 and semi-rigid coax cable W2. Relay K2 selects the YIG oscillator signal and applies it to the 2 to 12 GHz leveling module U5. A sample of the 8.000 to 11.999 GHz is coupled off leveler U5 and applied to relay K3 via semi-rigid coax cable W18. Relay K3 switches the signal to mixer U16 via semi-rigid coax cable W32. The 2.6330 to 3.9333 GHz (X3) Y1 reference oscillator signal is applied to the other input of mixer U16 via semi-rigid coax cable W12, transfer switch K1, coupler U13 and a male-to-male SMA connector.

4-78. Mixer U16 outputs a 99 to 198 MHz i f signal to the output PLL assembly A13 SMB connector J1 via coax cable W41. Assembly A13 provides the phase detection for the output PLL. The 99 to 198 MHz i f signal is referenced with the 10 to 19.9 MHz ÷ N signal from assembly A10 to generate the FM DRIVE signal. This FM DRIVE signal is applied to A9 YIG filter/driver assembly, which outputs the FM− drive at its pin 10 to YIG Y4, thus closing the 8.000 to 11.999 GHz output PLL.

4-79. 8 to 12 GHz Output Leveling Circuits

4-80. The 8 to 11.999 GHz output and leveling configuration is identical to the 2 to 4 GHz circuits described in paragraphs 4-55 through 4-60.

4-81. 12 TO 18 GHz BAND FUNCTIONAL OPERATION

4-82. 12 to 18 GHz Reference PLL

4-83. YIG oscillator Y1 outputs a 3.9663 to 5.9333 GHz (X3) signal. Operation of the 12 to 18 GHz reference PLL is similar to the 0.1 to 2 GHz reference PLL described in paragraphs 4-30 and 4-31.

4-84. 12 to 18 GHz Band Output PLL

4-85. Output YIG oscillator Y5 provides a 12.000 to 17.999 GHz signal to the 12 to 18 GHz leveling module U8 via isolator U7 and semi-rigid coax cable W5. A sample of the 12.000 to 17.999 GHz signal is coupled off U8 and applied to relay K3 via semi-rigid coax cable W3. Relay K3 selects and applies the signal via semi-rigid coax cable W32 to mixer U16. The 3.9663 to 5.9333 GHz (X3) Y1 reference oscillator signal is applied to the other input of mixer U16 via semi-rigid coax cable W12, transfer switch K1, coupler U13, and a male-to-male SMA connector.

4-86. Mixer U16 outputs a 99 to 198 MHz i f signal to the output PLL assembly A13 SMB connector J1 via coax cable W41. Assembly A13 provides the phase detection for the PLL. The 99 to 198 MHz i f signal is referenced with the 10 to 19.9 MHz ÷ N signal from assembly A10 to generate the FM DRIVE signal. This FM DRIVE signal is applied to A9 YIG filter/driver assembly, which outputs the FM− drive at its pin 12 to YIG Y5, thus closing the 12.000 to 17.000 GHz output PLL.

4-87. 12 to 18 GHz Output Leveling Circuits

4-88. The 12 to 17.999 GHz output and leveling configuration is similar to the 2 to 4 GHz circuits described in paragraphs 4-55 through 4-60.

4-89. Leveler U8 outputs via semi-rigid coax cable W19 to relay K4. Relay K4 provides the output switching via semi-rigid coax cable W8 to the 1 to 26 GHz coupler U2. The remainder of the configuration is as described in paragraph 4-58.

4-90. The configuration differs in that level control assembly A3 outputs the 12 to 18 GHz leveling signal at pin 7 which is applied via coax cable W50 to the 12 to 18 GHz leveler U8. The leveling signal biases a pin diode to attenuate the output of U8, thus maintaining a +5 dBm ±1 dBm leveled output into the step attenuator U23.

4-91. 18 TO 26 GHz BAND FUNCTIONAL OPERATION

4-92. 18 to 26 GHz Reference PLL

4-93. YIG reference oscillator Y2 outputs a 5.9663 to 8.6330 GHz (X3) signal via an SMA male-to-male connector to the 4 to 8 GHz coupler U1. The operation of the PLL is similar to the 0.1 to 2 GHz down converter PLL described in paragraphs 4-37 and 4-38.

4-94. 18 to 26 GHz Band Output PLL

4-95. Output YIG oscillator Y6 supplies a 18.000 to 26.500 GHz signal to isolator U10 via a male-to-male SMA connector. Isolator U10 outputs to the 18 to 26 GHz leveling module U11.

4-96. A sample of the 18.000 to 26.500 GHz signal is coupled off module U11 and applied to relay K3 via semi-rigid coax cable W5. Relay K3 switches the signal to mixer U16 via semi-rigid coax cable W32. The 5.9663 to 8.6330 GHz Y2 reference oscillator signal is applied to the other input of U16 via coupler U1, isolator U2, transfer switch K, semi-rigid coax cable W10 and coupler U13.

4-97. Mixer U16 outputs a 99 to 198 MHz i f signal to the output PLL assembly A13 SMB connector J1, via coax cable W41. Assembly A13 provides the phase detection for the PLL. The 99 to 198 i f signal is referenced with the 10 to 19.9 MHz ÷ 10 signal from assembly A10 to generate the FM DRIVE signal that outputs at A13 pin Y. This FM DRIVE signal is then applied to assembly A9 which outputs the FM− drive at its pin 12 to YIG Y6, thus closing up the 18.000 to 26.500 GHz output PLL.

4-98. 18 to 26 GHz Output Leveling Circuits

4-99. The 18.000 to 26.500 GHz output of leveler module U11 is coupled to the 18 to 26 GHz amplifier module U25 via a female-to-male SMA connector. U25 outputs via semi-rigid coax cable W38 to relay K4.

4-100. Relay K4 selects the 18.000 to 26.500 GHz output signal and routes it to the 1 to 26 GHz coupler U21 via semi-rigid coax cable W8. Output of U21 is directly coupled via an SMA male-to-female connector to the step attenuator U23. The step attenuator then outputs to the front panel RF OUT SMA connector J105.

4-101. A sample of the output signal is coupled off U21 detected by U22 and applied to A22 at connector U2. A logarithmic amplifier circuit contained in A22 converts the square-law detector output of U21, into a lin-log signal, and outputs at A22J3.

4-102. The level control assembly A3 receives the detector out signal from A22J3 via semi-coax cable W56 and generates the 18 to 26 GHz leveling signal. This leveling signal outputs an A3 pin 8 and is applied via semi-rigid coax cable W53 to the 18 to 26 GHz leveling module U11. The leveling signal biases a PIN diode to attenuate the output of U11, thus maintaining a +5 dBm ±1 dBm leveled output into the step attenuator U23.

4-103. CIRCUIT DESCRIPTIONS

4-104. Detailed circuit descriptions for this instrument are provided in the following paragraphs (4-105 through 4-254). Refer to chapter 7 of this manual for schematic and assembly drawing figures referenced in the circuit analysis that follows.

4-105. POWER SUPPLY

4-106. Model 1626 power supply provides the necessary fourteen regulated power sources for instrument

operation. It consists of various components, mounted at several locations within the main instrument chassis, along with A1 power supply heat sink assembly, which also mounts to the same main chassis (see figures 7-5, 7-6, and 7-7).

4-107. Power supply components, located on the main instrument chassis, include: front panel ON-OFF LINE switch, S101; rear-panel-mounted ac line filter/plug, J108, and main power fuse, F101; also, chassis-mounted power supply transformer, T1, total time (TT) meter, M1, power-line range select connector, J1/P1, thermal cutout connector, J2/P2, full wave rectifiers, U2 through U5, and single-stage filter capacitors, C1 through C7. Connector J3/P3 interconnects unregulated and regulated voltage levels to/from A1 assembly; while, connector J4/P4 outputs the remaining eleven regulated voltage levels. Varistors, VR1 and VR2, are connected across connector J1, pins 1 and 2, respectively, to ground potential for suppression of power-line transients. During 115-and 230-volt operation, varistor, VR1, is connected across transformer T1, primary: 100- and 200-volt operation utilizes varistor, VR2, also connected across the T1 primary. Plug, P1, wiring determines which varistor is connected into the circuit.

4-108. A1 power supply heat sink assembly mounts to the main instrument chassis by two #8 screws through mounting holes in the heat sink body. Attached to this assembly are the following components: three-terminal regulators, A1U1 through A1U11; capacitors, A1C1 through A1C22; 1.5 ampere MB fuses, A1F1 through A1F5; and thermal cutout switch (195° ±5° F), A1S1.

4-109. The three-terminal regulators, A1U1 through A1U11, provide voltage regulation and overload protection for each of the fourteen output voltage levels, one of which supplies the dc fan motor. Internal fuses, A1F1 through A1F5 (see table 2-2), furnish protection for the YIG devices in case of regulator failure and a subsequent overvoltage condition. (YIG devices are protected with zener diodes which conduct when overvoltage occurs, thus causing the protective fuse to open the defective output circuit.)

4-110. Model 1626 is shipped with a 2A, 3AG slow-blow fuse (main) for 100/115 V ac nominal operation. Should 200/230 V ac nominal operation be employed, the standard 2A, 3AG slow-blow fuse must be replaced with a 1A, 3AG slow-blow fuse to adequately protect the instrument. Line voltage selection, for operating in the ranges of 100 V, 115 V, 200 V, and 230 V ac nominal, is provided by connector J1/P1, which properly interfaces transformer, T1, multiple primary windings in accordance with actual ac line operating conditions. See figure 2-1 and table 2-1 for details concerning plug P1.

4-111. An overtemperature protection feature (thermal cutout switch, A1S1) is incorporated into Model 1626, which removes ac line power from the instrument, if internal overheating occurs. This thermal switch is mounted on A1 heat sink assembly, along with fuses A1F1 through A1F5. If the instrument should overheat, causing switch A1S1 to open, a waiting period of approximately one-half hour to one hour will be necessary before automatic power reset occurs. This waiting period may be shortened by removal of the top cover panel for accelerated cooling.

NOTE

Overheating/power shutdown may be an indication of excessively warm, rack-cabinet air; external air-flow obstructions; or dirty fan filter. When power is reapplied, be certain that the instrument fan is functioning properly.

4-112. A2, IEEE 488 PCB ASSEMBLY

4-113. The function of this pc board is to control and process the data transferred from IEEE 488 communications bus to the Model 1626. See figures 7-8 and 7-9 . Microprocessor, U6, the MC6802, is the central processing unit (CPU) of this board. Information is received and transmitted via data bus lines, D7 through D0 (U6 pins 33 through 26). This data is directed to the receiving device by address bus lines, A15 through A0 (U6 pins 25 through 22, and 20 through 9).

4-114. The direction of data transfer is controlled by the read/write (RW) line (U6 pin 34). A logic "high" indicates that the CPU is receiving (i.e. reading) data, and a "low" indicates that another device is receiving data (i.e., the CPU is writing data to that device). The enable (E) line (U6 pin 37) synchronizes the information flow to and from the CPU.

4-115. Decoding of the address lines at U8 utilizes address lines A15, A14, and A13; also, valid memory address (VMA) line (U6 pin 5), to generate the three strobes required by the system. These strobes are identified by mnemonics ROMSL, GP488, and GPIA1. Strobe GPIA2 is not utilized since U12 is an optional expansion and is not included in this system.

4-116. The most significant address strobe from U8 is ROMSL (pin 4). It controls the access to read-only-memory (ROM) U7. This ROM provides the CPU with the programming necessary for its functions. Strobe GP488 allows access to U4, the IEEE 488 interface control IC. Strobe GPIA1 allows access to U13, the peripheral interface adaptor (PIA).

4-117. The remaining address lines from the MC6802 are used primarily to select the appropriate ROM addresses. Only address lines A2, A1, and A0 (U6 pin 11,

10, and 9) are connected to the other peripheral devices as required. They control internal functions within those ICs and will not be discussed here.

4-118. IC, U4, the MC68488, controls all of the interface activities associated with the IEEE 488 bus. The three wire handshake, using lines DAV, DAC, and RFD (pins 16, 17, and 18), is completed internally. Whenever the IEEE 488 bus requests service (e.g. talk, listen, remote-local change of state), the initial byte from the bus causes an interrupt request, driving the IRQ line (pin 4) "low". The IRQ LED will flash, giving a visual indication of this situation. This is a momentary change, however, as the CPU will respond to the interrupt, thus clearing the IRQ line. Each additional event occurring in the data transfer sequence is handled without involving the IRQ line.

4-119. The PIA, U13, buffers data transmitted to frequency, level, and mode control circuitry in the Model 1626. The sixteen available data transfer lines are configured by the system software as six inputs and ten outputs.

4-120. The inputs are the synthesizer data addresses D through A (pins 5 through 2), the LOCK line (pin 8), and the LEVEL line (pin 7). These lines allow the CPU to ascertain which data to transfer at any particular instant, and allow sensing of the instrument condition by the system controller, via the IEEE bus.

4-121. The synthesizer data addresses are controlled by the WAIT output line (U13 pin 6). In remote operation the WAIT line is set "low" only during the transfer of data to the synthesizer. In local operation the WAIT line is "high." Frequency data outputs appear on pins 13 through 10, and level data outputs on pins 17 through 14.

4-122. A3, LEVEL CONTROL PCB ASSEMBLY

4-123. The level control system (see figures 7-10 and 7-11) rf output of the instrument, with a detector diode, amplifies this voltage, compares it to a setpoint voltage, and produces an error signal controlling a leveling element which varies the rf signal seen by the detector diode, in such a manner as to decrease the amount of error signal. Feedback, thus controls the level of the rf signal in a manner proportional to the setpoint signal.

4-124. Level control, A3, processes frequency and output level information and corrects for any variations in the microwave components which are a function of frequency, attenuator settings, modulation characteristics, or temperature. It provides a signal representing the output power of the instrument and certain modulating signals. Its functions can be divided into six basic blocks.

4-125. Error Correction Circuits

4-126. This block generates an error correction voltage proportional to the difference between the insertion loss at the calibration frequency and the operating frequency of the instrument. Data representing the attenuator setting, is presented to U2 which converts this to binary-coded-decimal format. IC, U4, selects between front-panel and remote attenuator (option 02) data. Attenuator setting and frequency data address PROM U6, describes variations from the ideal for each of the attenuator's 10 dB steps. Frequency data addresses for PROM U5, describes differences between the uncorrected power output and the desired power output. IC, U1, converts the 1− and 10− GHz frequency information to binary format to permit installation of smaller PROMS.

4-127. The outputs of U5 and U6 are summed by adders U7 and U8.These are presented to DAC U9 which produces a current proportional to the digital input. IC, U18-1, converts this current to a voltage. IC, U18-7, produces a reference voltage for U9 and other circuitry.

4-128. Level Control Circuits

4-129. This block provides proper scaling of the correction voltage input, generates the setpoint voltage for the level control function, and scales the input of the microwave level detector. The amplified detector output from video amplifier, A22, is amplified by U25-8 and U25-1. Transistor, Q11, and IC, U36-14, select this signal in CW mode. Calibration of the rf output level at 0 dB and 9 dB attenuation (+5 and −4 dBm) is provided by R34 and R36 (1-26 GHz), or R33 and R37 (0-1 GHz); as selected by Q13 and U36-8, or Q14 and U36-7. The signal is amplified by U25-14 and sent to a logarithmic amplifier composed of Q23, U16, and U17. This circuit converts the detector signal into a voltage scaled at 0.1 V/dB.

4-130. IC, U18-14, amplifies the correction voltage produced by U18-1. Resistor, R7, scales this voltage to 1.000 V/dB correction. The setting of R7 is critical if accurate power level is to be maintained, as all system characterization data is scaled by this one adjustment. Resistor, R9, is an offset adjustment which centers the output of U18-14 and the following amplifiers to a level compatible with output of the log amplifier.

4-131. ICs, U11 and U12-1, generate a voltage indicating position of the 1 dB attenuator switch, and either the front-panel vernier or the remote vernier, as selected by U15-8. Resistor, R10, scales the output of U12-1 to 1.0 V/dB. IC, U24-1, converts the remote vernier current to a voltage. The outputs of U18-14 and U12-1 are scaled to 0.1 V/dB by U12-8 and U13-14 to provide the setpoint voltage for U14-14.

4-132. IC, U14-14, generates an error signal when the setpoint voltage from U13-14 and the processed detector voltage from U16-6 are not identical. Transistor, Q8, is a switch which controls the circuit-gain bandwidth characteristics. A lower bandwidth is required in pulse operation since the minimum pulse rate is 100 Hz. This error signal is sent to U14-1 which drives an exponential amplifier, formed by Q9 and Q10. This circuit keeps the gain of the leveling loop more nearly constant by compensating for the nonlinear characteristics of the leveling diodes.

4-133. IC, U14-7 and transistor, Q4, buffer the output of the exponential amplifier and provide high-current drive to the PIN leveling diodes in the three leveling modules U5, U8, and U11. The rf output level is sensed by microwave detector diodes U20 (0 to 1 GHz) or U22 (1 to 26 GHz); amplified by video amplifier, A22, and sent to level control, A3, thus closing the leveling loop.

4-134. Pulse Generation and Selection Circuits

4-135. This block generates the variable-rate square-wave modulation signal and selects the signal used to pulse modulate the unit.

4-136. ICs, U26 through U31, form a logic network which selects either a fixed-rate square wave; a variable-rate square wave; a variable-rate, variable-width pulse; a fixed-rate, fixed-width pulse; or an external pulse source as the modulating signal for the unit. The fixed-rate signals are generated on frequency control, A7. Only the fixed-rate signals and external pulse inputs are available in remote operation.

4-137. IC, U33, is an astable multivibrator operating from 200 Hz to 100 kHz. IC, U32-12, divides this frequency to produce 100 Hz to 50 kHz. This signal is sent to sweep control, A4, where it triggers a pulse generator which produces pulses that are variable in width from 0.1 to 10 microseconds. Either this pulse, or the square wave is returned to the selection logic described above. The modulating waveform, regardless of its source, eventually appears at U29-11 and drives modulator assembly, A27. This turns on the PIN modulating diodes in leveling modules U5, U8, and U11 to greatly attenuate the output signal, thus producing pulse modulation. In CW mode, this line is pulled "low" by U31-6 and CR7 to reverse-bias these diodes and minimize the insertion loss of these modules.

4-138. Pulse Sampling Circuits

4-139. These circuits sample the rf output power level during pulse operation in order to provide proper leveling during pulse modulation. The modulating waveform from U29-11 is inverted by U27-11 and buffered by U29-6. It triggers one-shot multivibrator, U34-13, which compensates for circuit delays and the risetime of the rf output pulse. IC, U34-5, 12 produces two complimentary pulses which drive a sampling circuit composed of Q15, Q16, Q17, Q18, CR8, CR9, CR10, and CR11. The detector output voltage is thus sampled for approximately 70 nanoseconds after the rf output pulse has reached its final value. Resistor, R44, balances the sampling bridge. Capacitor, C22, stores the sampled detector voltage. IC, U35-1, buffers this voltage to minimize loading on the capacitor.

4-140. IC, U35-7, amplifies the output of U35-1 and drives three networks which calibrate the peak rf output power at 0 dB and 9 dB attenuation for the leveling modules. Resistors, R21 and R24, are selected by Q7 and U24-14 (0 to 12 GHz); R22 and R25 by Q5 and U24-7 (12 to 18 GHz); R23 and R25 by Q5 and U24-8 (18 to 26 GHz). The signal is then amplified by U25-7 in pulse mode. Operation, thereafter, is identical to CW mode, as described above.

4-141. Temperature Compensation Circuits

4-142. This block provides compensation for temperature variations of the detector diodes. IC, U19, is a temperature-sensing device which outputs 10 mV/° K. IC, U13-1, amplifies this voltage to 200 mV/degree. Resistor, R27, is an offset adjustment used to set the output of U13-1 to 0 V at 25° C. Resistors, R29 and R35, are silicon, temperature-sensitive resistors with a positive, nonlinear temperature coefficient. These resistors vary the gain of U13-8 and U13-7, and provide an output voltage which is summed with the correction and 1 dB attenuator voltages by U12-8. This voltage compensates for the temperature behavior of detector diodes, U20 and U22.

4-143. Display Driver Circuits

4-144. This block generates the signal which drives the front panel, power level display. ICs, U10 and U12-7, generate a voltage, indicating the position of the 10 dB attenuator. Resistor, R13, scales this voltage to 0.1 V/dB. The outputs of U12-7 and U12-1 (1 dB attenuator and vernier settings, scaled to 1.0 V/dB) are summed by U12-14. This voltage indicates the desired power output level. Resistors, R15 and R14, are gain and offset adjustments for U12-14 and calibrate its output for proper indication of the power display. The output of U12-14, or the output of power meter, A8, (from the front-panel, power meter input) is selected by U15-16, 3, and sent to power display, A15, which displays either the rf output level of the instrument or the power applied to detector diode, U103.

4-145. A4, SWEEP CONTROL PCB ASSEMBLY

4-146. The major functions of this unit are to generate the sweep timing and control signals, the sweep ramp, and to process the remote amplitude

and mode control data. The pulse-width control circuit is also on this board. See figures 7-16 and 7-17.

4-147. The 10 MHz input on pin 3 is divided by U13 to produce a 1 MHz signal, which is further divided by U1 and U2 to produce 250 kHz. The 250 kHz signal is divided by U14 to produce 25 kHz. Counter, U22, will receive a clock signal at 250 kHz, if the front-panel sweep rate is set to 1 kHz; at 25 kHz, if the sweep rate is set to 100 Hz; and 250 kHz gated by U2 (pins 1, 2, and 3) in the single-step mode.

4-148. The 10 kHz input on pin L is divided by U36 to produce 1 kHz and 100 Hz outputs. Depending on the sweep rate selected, one of these signals is gated by U35 and U19 to pin P, except in single step mode. This is the COUNT output and it is fed to the frequency control board where it increments the Model 1626 output frequency, 1 MHz, each time it occurs.

4-149. The level of the SWEEP OUT ramp must increase linearly with the number of COUNT pulses, independent of sweep width. This ramp must be 0 V at the beginning of each sweep and 10 V at the end of each sweep. The 10 V level coincides with the last COUNT output pulse. This is achieved by using an 8-bit presettable counter, composed of U17 and U18, which drives digital-to-analog converter (DAC), U6. The circuitry is arranged such that, at the beginning of a sweep the bcd counter output is 5, and at the end of sweep the bcd counter output is 255, scaled to give a 0-10 V SWEEP OUT output signal.

4-150. If the required sweep width is 10 MHz, then 10 COUNT pulses would correspond to one sweep (since 1 pulse at the COUNT output corresponds to a 1 MHz increase in output frequency). For the SWEEP OUT signal to increase linearly with the number of COUNT pulses, the 8-bit counter must receive 25 clock pulses per COUNT pulse. Similarly, if the required sweep width had been 1000 MHz, the counter must receive 0.25 clock pulses per COUNT pulse.

4-151. The counter clock pulses are generated as follows: the digital sweep width data is fed to four-stage, presettable bcd counter, U22 through U25. These integrated circuits are connected as ripple, down counters. When all counters are at 0, the sweep width data is reloaded and a new count begins. IC, U22, receives a clock-pulse rate of 250 times the count-pulse rate, therefore, if a sweep width of 10 MHz is set (corresponding to 10 COUNT pulses) this four-stage counter will go through 25 count cycles per COUNT pulse. Ten count pulses will be required to complete the sweep, corresponding to 250 output pulses from the four-stage counter. This gives the required scaling for the SWEEP OUT signal, as a function of sweep width.

4-152. Another facility of the instrument is to have single step control in the SWEEP mode. This is accomplished as follows: when in the STEP mode, the 1 kHz and 100 Hz select lines are "low". In this condition, U2 (pins 8, 9, 10, 11, 12, and 13) inhibits the clock signal to U22. When the front-panel STEP switch is actuated, U5, a dual D-type flip-flop, is used to debounce this input. The Q output (pin 5) goes "high", thus giving a COUNT pulse via U19 (pins 1, 2, and 3), and gating the 250 kHz clock signal to U22 via U2 (pins 1, 2, and 3).

4-153. This pulse also loads counters, U3 and U4, which count 250 pulses before the RC output of U4 (pin 13) goes "low". This causes U5 to reset, so that the 250 kHz clock pulses to U22 are again inhibited. In this cycle, the four-stage counter has received 250 clock pulses for one output COUNT pulse, exactly the same as when operating in the automatic SWEEP mode. The SWEEP OUT signal will, therefore, be similarly scaled. When a sweep cycle is completed, it is necessary to reset U1, U14, U22 through U25, and to load U17, and U18, before another cycle commences.

4-154. This is done as follows: assume the instrument to be in SWEEP mode. COUNT pulses at one shot, U11 (pin 4), have no effect on this circuit while U11 (pin 5) is "low". When counters, U17 and U18, reach maximum count, pin 12 on these integrated circuits will go "high", providing a "high" at U11 (pin 5). IC, U11, will now trigger on the next COUNT pulse. IC, U11 (pin 6), will then set D flip-flop, U34, via U19; U10 (pin 13) will go "low" and U10 (pin 1) will go "high", thus resetting and loading the appropriate circuits. If the instrument is in 1 STEP mode, U10 (pin 13) going "low" would send U16 (pin 3) "low", thus resetting U34. IC, U11, is present to reset the system whenever the mode of operation is changed.

4-155. The PEN LIFT output is provided by Q1, giving an inverted form of the output signal on U10 (pin 1). The PRESET output is provided by U16 (pin 6), giving a buffered version of the output signal on U10 (pin 1). A 1 kHz output is provided on pin 20.

4-156. When in the CW mode, or when RESET is pressed, U19 (pin 8) is "high", thus holding the circuit in the reset condition. It is necessary to bypass microwave YIG filter, FL1, when in the SWEEP mode, since in this condition, it cannot track properly. This is achieved by one of U38 outputs activating relay, K7, on the microwave deck. The other outputs of U38 are for options not present in this instrument.

4-157. The remainder of the sweep control board consists of the remote interface for amplitude and mode control. Latches, U27 through U30, decode and store the data from frequency control board, A7. The 10-dB data outputs are only used with an optional 10-dB attenuator control, not present in this instrument. Multiplexer, U31, selects either local or remote 1-dB data. The vernier overrange signal is produced by DAC, U9. Decoder, U8, produces control signals to remotely select the modulation mode. Decoder, U33, produces the SWEEP mode signals and multiplexer,

U32, selects local or remote. Flip-flop, U34, debounces the front-panel, single-step button. The remaining circuit Q2, Q3, U12 produces a variable-width pulse from the pulse-rate signal at pin 19. IC, U12, selects either this pulse or the input square wave.

4-158. A6, OSCILLATOR DRIVER PCB ASSEMBLY

4-159. The purpose of this board is to generate relay drive for the microwave switches; the frequency band information required by other boards; the main tuning currents for the microwave oscillators; and the bias voltages necessary to operate Gunn diode oscillators. See figures 7-26 and 7-27.

4-160. The bcd information, defining the 1s and 10s GHz frequency setting, is buffered by U18 and U8, and used to address PROMs, U10 and U17. These integrated circuits decode the data to produce outputs which indicate the band in which the selected rf frequency falls. These outputs are available for other boards that require frequency band information. IC, U7 and U14, operate the relays controlling the microwave switches. The outputs of U10 and U17 are also used elsewhere on the oscillator driver board.

4-161. The bcd information defining 1s GHz and 100s MHz frequency settings are fed into digital-to-analog converter (DAC), U19. The DAC gain, and the gain of operational amplifier, U3, are adjusted to give a voltage at TP1 of 250.0 mV/GHz. Resistor, R52, provides offset adjustment. The high-precision reference voltage for U19 is generated by precision voltage regulator, U12.

4-162. To obtain the required resolution, the DAC converter is only used to convert the second and third most significant digits of output frequency. An output frequency change of 100 MHz corresponds to a 25 mV change at TP1. If the DAC had been used to convert three digits, the least significant digit resolution at TP1 would be 2.5 mV, which is an unreliably small voltage. For this reason, the most significant digit information (10 or 20 GHz) is converted using Q1 and Q2 and the summing junction of U3; the weighting being controlled by the matched resistors, A6A1R1 and A6A1R2, and resistor, A6A1R3.

4-163. The DAC offset circuit operates as follows: the output voltage of U13 (pin 14 of the output oscillator) is required to be 0 V at the bottom end of each oscillator range (e.g. 2.000 GHz for the 2-4 GHz oscillator, etc). FETs, Q3, Q4, Q7, Q8, Q9, and Q11, are controlled by the frequency band signals from U10 and U17; only one device will be ON for any frequency.

4-164. Variable resistors, R53 through R58, are adjusted so that the negative voltage being summed into U13 by this circuit is exactly equal to the positive voltage from U1, at the bottom end of each oscillator frequency band. FETs, Q5, Q6, and Q10, operate in exactly the same way for the reference oscillator.

4-165. The 10s MHz and 1s MHz information is converted to a voltage by a DAC on frequency control board, A7, and is summed into U13 (pin 13) via U13 (pins 5, 6, 7). The output, U13 (pin 14), feeds FET switches, Q21, Q22, Q26, Q27, Q28, Q29, via variable resistors, R74 through R79, and fixed resistors, A6A4R1 through A6A4R6. These FETs are controlled by the outputs of U17 in the same way as in the DAC offset circuit.

4-166. Control of the main tuning current for the microwave oscillators is obtained as follows: the tuning current for the output oscillator is proportional to the voltage at U24 (pin 6). If the selected frequency is 2 GHz, this voltage will be set by R70 via Q13 (although Q22 is on the output at U13, pin 14 will be 0 V). The output frequency of the oscillator is set to 2 GHz by varying R70. As the selected frequency is increased, the output voltage on U13 (pin 14) will increase at a rate of 250 mV/GHz. When this voltage reaches 1.975 V, the oscillator output frequency must be 3.9 GHz. This frequency is obtained by adjusting R79. The oscillator main-tune driver is now calibrated for the 2-4 GHz oscillator. The remaining output and reference oscillators, and associated drive circuits are calibrated in exactly the same manner.

4-167. Pin 12 of the pc board is connected to the gate of the oscillator driving FET. The output on U24 (pin 6) must be filtered before driving the FET, to reduce noise on the signal. However, the oscillator must also be capable of rapid frequency changes when operating in the SWEEP mode and the presence of a low-pass filter prior to the gate of the FET would impede this capability.

4-168. These apparently conflicting requirements are satisfied as follows: under steady-state conditions the oscillator frequency will be stable and the voltage on U24 (pin 6) will be constant. The gate of the FET has a very high impedance; therefore, no voltage will be dropped across R19, and transistors, Q30 and Q32, will be off. When any relatively fast transients occur on U24 (pin 6), C12, C13, and R15, will provide a low-impedance path to ground, relative to 100 kΩ. Depending on the sense of the transient, the voltage dropped across R19 will then turn on the appropriate transistor, providing a low-impedance driving path to the FET gate. The same bandwidth-switching circuit is used in the reference oscillator drive circuitry, except for a slightly higher value for R16.

4-169. The oscillators covering the frequencies from 2 to 8 GHz are YIG-tuned oscillators which operate from constant supply voltages. A simple regulated power supply is sufficient for oscillators of this type. The oscillators covering the 8-12 GHz, 12-18 GHz, and 18-26 GHz frequency bands may be YIG-tuned or Gunn diode oscillators.

4-170. Gunn diode oscillators require a power supply voltage which varies inversely with the frequency of oscillation. This voltage is provided as follows: the buffered DAC voltage on U1 (pin 6) is further buffered by U26 (pin 14). Assume the output frequency to be in the 8-12 GHz region. IC, U10 (pin 4) and U8 (pin 14) will be "high", the latter being approximately 14 V. This voltage is applied to the junction of diodes CR32 and CR42, reverse biasing both elements.

4-171. The voltage on U26 pin 5 is therefore equal to the "+R" reference voltage generated by U6. The voltages at U26 pin 7 and U28 pin 2 will now be a function of the voltage on U26 pin 14. The V_b sense line, pin B, performs remote sensing of the oscillator supply voltage, and is connected to the V_b supply pin of the appropriate oscillator. This completes the feedback loop for U26 pin 7.

4-172. The voltage appearing on pin F is the output of a variable-voltage regulator mounted on the instrument rear panel. The output of this regulator is controlled by the voltage on U28 pin 1, which appears on pin J of the board.

4-173. When the 8 to 12 GHz frequency range is not selected, the junction of diodes, CR32 and CR42, is held to approximately −14 V. This causes Q36 to turn off and reduces the voltage at U26 pin 5 sufficiently for the output to be fixed at the negative supply voltage. This forces the regulator to 0 V output. The drive circuits for the 12 to 18 GHz and 18 to 26 GHz oscillators operate in an identical manner.

4-174. A7, FREQUENCY CONTROL PCB ASSEMBLY

4-175. The frequency control board processes the frequency select data from either the front-panel lever switches or the IEEE 488 interface pc board, demultiplexes, and stores this information in a register which may be incremented to provide the SWEEP function. Additional circuitry provides lock detectors, status lamp drivers, a calibrated pulse, and an analog output proportional to the 1 and 10 MHz digits. See figures 7-29 and 7-30.

4-176. Input data is switched by U18 and applied to latches, U2 through U4, and U12 through U17. These latches are strobed at the proper time with signals produced from U5. The input to U5, from counter U7, is gated by U6 and counter, U19, to provide a narrow pulse. The outputs from the latches are used to preset a five stage counter. The load and clock lines are controlled by the sweep control board, A4, to increment the counter when in the SWEEP mode.

4-177. Adders, U22 and U23, produce an offset when the below 2 GHz portion of the range is used, so that the 8 to 12 GHz oscillator may operate at the appropriate frequency. Resistors, R22 through R30, perform level translation for ECL compatibility.

4-178. A current proportional to the 1s MHz and 10s MHz digits, is produced by DAC, U1, for use by the oscillator driver assembly, A6. This current appears on pin 7.

4-179. The individual lock indicator signals are monitored by comparators, U9 and U10. If an out-of-lock voltage level is sensed, the corresponding indicator will illuminate and the lock status will change appropriately. Transistor, Q1, drives the lock indicator on the front panel. Transistor, U2, and two sections of U10, provide level indication drive.

4-180. Flip-flops, U20/U21, and exclusive-OR gate, U30, produce a pulse train with a 1 microsecond wide pulse at a 1 kHz rate.

4-181. A8, POWER METER PCB ASSEMBLY

4-182. This circuit provides an output voltage proportional to the logarithm of the input power (i.e., the output voltage is directly proportional to the input power in dBm). See figures 7-31 and 7-32. The front-panel power meter detector output is connected to pin X on the pc board, where it is filtered by R2 and C1 and amplified by U1. U2 is a unity gain stage providing a dc offset facility for calibration. U3 converts the processed detector voltage to its (base-10) logarithm. Due to the limitations of the detector, compensation is required when measuring power levels over a 40 dB range.

4-183. This wide range power level compensation is provided by the diode/resistor network around U4. The 0 dB adjustment potentiometer R40 and the +10 dB adjustment potentiometer R24 provides for the calibration of the specific detector diode used in the instrument.

4-184. A9, YIG FILTER/FM COIL DRIVER PCB ASSEMBLY

4-185. This circuit tunes the 2 to 12 GHz YIG filter to the instrument selected output frequency and provides voltage to current conversion to drive the fm coils of the microwave oscillators so that frequency lock may be obtained. See figures 7-33 and 7-34. The D/A voltage at pin F is generated by the oscillator driver assembly from the 10s GHz, 1s GHz, and 100s MHz, frequency digits. This voltage changes at a rate of +250.0 mV/GHz. The 10 MHz D/A voltage at pin B is generated by the frequency control assembly, A7, from the 10s MHz and 1 MHz frequency digits. This voltage changes at a rate of −50.0 V/MHz rate . The D/A voltage is inverted by U2 and summed with the main D/A voltage by U3.

4-186. The 1000 pF capacitor across U3 causes the frequency response of the YIG filter driver portion of the circuitry to decrease at a rate of 6 dB/octave. R9, R12, and C9, provide an additional RC roll-off pole. The bandwidth of the driver is kept narrow unless a fast change of frequency is needed. In this case, the transient voltage drop across R9 turns on transistor, Q7, effectively removing the second RC pole.

4-187. U1, enables the YIG driver circuitry to the YIG filter from 0 to 12 GHz. Above 12 GHz, the driver is switched out and the YIG filter has a fixed idle current which tunes it to approximately 2 GHz.

4-188. The fm tuning coils of the 2 to 4 GHz, 8 to 12 GHz, 12 to18 GHz, and 18 to 26 GHz oscillators are driven in series from pin B. The 4 to 8 GHz oscillator is driven separately and switched out when it is being used for a reference oscillator. U1 performs this switch-ing function.

4-189. The output at pin 17 is a correction voltage from the output PLL. This level is summed into the output driver to increase the capture and hold-in range of the output PLL assembly, A13.

4-190. A10, OUTPUT DIVIDE-BY-N PCB ASSEMBLY

4-191. This circuit divides the i f signal by a preset number N, to provide a reference frequency for the output PLL assembly, A13. See figures 7-35 and 7-36. Q1 and associated components form a VCO which operates from 100 to 200 MHz.

4-192. The programmable prescaler, U7, prescales by either 10 or 11 depending on the state of the Set P input, U7 pin 2. U6 and U5, are bcd counter latches and U1, is a simple flip-flop. At the beginning of every count cycle, U1 is preset to 1.

4-193. The count in U6 remains at zero when the prescaling number P changes from 11 to 10. This is accomplished by U2 pin 15 which disables U6 by setting U6 pin 10 from low to high. The output of U2 also changes the state of U7 pin 2.

4-194. When the outputs of U5 and U1 pin 2 are zero an output pulse is generated by the zero-count sensor composed of U2 pin 3 and U1. This occurs after 136 input pulses. The signal from U1 pin 14 changes state and allows the loading of the preset information into U6 and U5, and forces U1 pin 2 to a set state. Since the counts are no longer all at zero, the cycle will repeat again. The net result of this circuit is to produce one output pulse for each group of N input pulses (thus the name divide-by-N.)

4-195. The zero-count pulse from U2 pin 3 is also applied to phase detector, U3. The other input to U3 is a 1 MHz reference signal which is converted to appropriate ECL levels by C7, R20, and R22. The output of the phase detector feeds differential amplifier, U4, which converts the pulsed output of the phase detector to a filtered signal suitable for driving the VCO. Diodes, CR3 and CR4, connected to the output of the phase detector via 1 k resistors, provide the lock detector signal which is fed to frequency control assembly, A7.

4-196. U8 divides the VCO signal by a factor of 10 to generate the final output of the board. The VCO operates at 100 to 199 MHz to keep the acquisition time low, thus allowing the oscillator to react quickly to any error detected by the phase detector.

4-197. A11, FIXED LO PCB ASSEMBLY

4-198. This circuit provides a main tuning current and phase detector circuitry to tune the 4 to 8.7 GHz oscillator operating at 8.001 GHz. This frequency is used as the local oscillator for mixer U17 when in the 0.1 to 2.0 GHz range. See figures 7-37 and 7-38. Sampling mixer, A20, produces a comb line at 8.000 GHz which mixes with the 8.001 GHz frequency of the oscillator to produce an intermediate frequency output of 1 MHz. The output stage of sampler, U15, consists of a FET in the open drain configuration. The drain of this FET feeds into pin B of the PC board thus providing a current path for transistor, Q4, and forming a cascade amplifier. This circuit has a nominal bandwidth of dc to 20 MHz.

4-199. The collector of Q4 drives transistor, Q5, which is a unity gain buffer. The emitter of Q5 is ac coupled to an impedance matching circuit, R1 and C1, the output of which drives a 3 stage filter. The 3 dB cutoff frequency of this filter is 20 MHz with a notch at 33.33 MHz which serves to filter out any sampling frequency feedthrough from the sampler. U1 is an ECL line receiver which contains 3 amplifiers. This circuit provides approximately 45 dB gain.

4-200. Phase detector, U2, compares the frequency of U1 output with a 1 MHz reference signal. The filtering action of R15, C13, R16, and C12, provides some integration of U2 outputs, which are then fed to differential amplifier, U3. The output from U3 pin 1 passes through a notch filter centered at 1 MHz.

4-201. When the frequency of the instrument is in the 0.1 to 2.0 GHz band, switch, U6, will be closed and the output of the notch filter will feed transistors, Q1 and Q2, a high-gain discrete Darlington configuration. The output of Q2 supplies the fm coil tuning current of the 4 to 8 GHz oscillator thus completing the phase detector loop. Amplifier, U3 pin 7, is present to ensure that the loop locks at an output frequency of 8.001 GHz. When the system is activated, the start-up frequency of the YIG oscillator may be anywhere within its band.

4-202. If the oscillator frequency is higher than 8.001 GHz the intermediate frequency of sampling mixer, U15, will be greater than the 1 MHz reference

frequency. The output of the phase detector under these conditions will cause U3 pin 3 to change so as to reduce the frequency of the oscillator until the loop locks. Should the oscillator frequency be less than 8.011 GHz but greater than 7.999 GHz, the sampling mixer i f signal will be in the 0 to 1 MHz region. Under these conditions, the phase detector will reduce the output voltage of U3 thus increasing the oscillator frequency until the loop locks.

4-203. If, however, the oscillator frequency at turn on should be less than 7.999 GHz, the output of the sampling mixer will be greater than the 1 MHz reference frequency. Under these conditions, the voltage at U3 pin 1 will increase, thus decreasing the oscillator frequency still further. The voltage at U3 pin 1 will eventually approach its positive supply voltage, holding the oscillator at some arbitrarily low (and incorrect) frequency.

4-204. To avoid this condition, U3 pin 7 is present. If the output of U3 pin 1 should exceed +11.2 V, it is assumed that the loop is not locked but in the condition described in the paragraph above. Under these conditions, U3 pin 7 will go negative, reducing the voltage at U3 pin 3 until it becomes less than that of U3 pin 2. U3 pin 1 will rapidly approach the negative supply voltage and U3 pin 7 will change state, thus disconnecting itself from U3 pin 3. Meanwhile, the output of U3 pin 1 is coupled through Q1 and Q2 to the microwave oscillator, whose frequency will change to greater than 7.999 GHz.

4-205. ICs, U4 and U5, are open-collector comparators which provide an out-of-lock indication whenever the control voltage from U3 pin 1 exceeds the limits set by resistors, R31, R32, and R33. It is assumed that the voltage will be within these limits if the loop is locked.

4-206. The required main tune current for the 4 to 8.7 GHz oscillator is provided by transistor, Q3, which in turn is controlled by amplifier, U7, in a closed loop feedback circuit. Zener diode, VR1, provides a voltage reference, and variable resistor, R38, provides a small adjustment of the main tune current to ensure that the frequency of the oscillator is within the capture range of the phase-locked-loop circuit on this board.

4-207. A12, 33.33 MHz REFERENCE PCB ASSEMBLY

4-208. This assembly generates a 33.33 MHz reference which is phase locked to either the internal reference or to an external time base. This latter function is not used in the Model 1626. Reference signals at 10 MHz, 1 MHz, and 100 kHz are also produced. See figures 7-39 and 7-40. The internal 10 MHz signal at pin M or the amplified 10 MHz from pin K is selected by U5. Switching is automatic and occurs whenever a sufficient signal is present at pin K (and thus the external input). Amplifier, Q2, and inverter, Q3, supply proper switching signals from the voltage supplied by detector, CR2. The output of U5 pin 3 feeds a divide-by-3 counter to provide a 33.33 MHz reference to phase detector, U3. IC U45 pin 3 also feeds counters, U6 and U7, which give the 1 MHz and 100 kHz outputs.

4-209. Differential pair, Q4, Q5, crystal Y1, and tuning diode, CR5, provide the basis of the VCO which, when locked to the reference input, will provide the 33.33 MHz output. After buffering via Q6, the VCO output is inverted by Q7. The collector of Q7 feeds a divide by 10 counter, U2, which drives input R of the phase/frequency detector.

4-210. Phase detector, U3, produces pulses proportional to the frequency difference between the two input signals. A lock detector formed by CR3 and CR4 sense the presence of large pulses to indicate an unlocked condition. U1 integrates the output of U3, and supplies gain and compensation to drive tuning diode CR5, thus controlling the frequency. Two 33.33 MHz outputs are required to drive samplers A19 and A20. These are found on pins B and C.

4-211. A13, OUTPUT PLL PCB ASSEMBLY

4-212. This circuit generates the required fm tuning current to lock the output oscillator. See figures 7-41 and 7-42. The amplitude of the output from mixer U16 will vary with frequency for three main reasons; first, the mixer response is not entirely flat over the band of interest; second, depending on the instrument output frequency the output of PLL may be locking on either the fundamental or the third harmonic of the reference oscillator signal; and third, the power of the output and reference oscillators vary with frequency.

4-213. These variations can result in as much as 40 dB of change in the output amplitude of the signal. It is therefore necessary to use an automatic level control circuit to ensure that the signal applied to divider, U6, remains within ECL compatible levels.

4-214. This is achieved by using four fixed gain amplifiers, U1, U2, U3, and U4, which provide approximately 40 dB total gain, and four PIN diode attenuators. The rf resistance of these diodes is varied by controlling the dc current flowing through these units. By monitoring the amplitude of the output signal at U4 pin 2, attenuation of the units can be controlled to maintain the output signal constant in amplitude.

4-215. Diodes, CR4 and CR5, detect the level of the output from U4 pin 2. This voltage is buffered by U4 pin 7. IC, U5 pin 1, sums this signal with a fixed dc offset. The output of U5 pin 1 drives the base of Q1, which controls the dc current through the PIN diodes, and thus attenuates the rf signal being amplified.

4-216. If the rf level is too high, the output of U5 pin 7 will be more positive than the dc offset. This will

drive U5 pin 1 negative, decreasing the PIN diode current, increasing rf resistance and attenuating the signal. Conversely, if the rf level is too low, the output of U4 pin 7 will be lower than the dc offset, causing U5 pin 1 to go positive; the diode current will increase, decreasing attenuation and thus increasing the amplitude of the signal. In either case, the attenuation will be changed to provide an appropriate signal level.

4-217. IC, U6, divides the input signal by a factor of 10. IC, U7, compares the relative frequency of the output of U6 with the output of the output divide-by-N assembly, A10, (which is 100 to 199 MHz divided by 10). The output of this unit is processed by U8 and sent to YIG filter/fm coil driver assembly, A9, where it controls the output frequency of the output oscillator. ICs, U9 and U10, provide a lock detector circuit. Operation of these units is identical to the similar circuit on the fixed LO assembly.

4-218. A14, REFERENCE PLL PCB ASSEMBLY

4-219. This circuit generates the fm tuning current required to lock one of two microwave oscillators used as a reference source within the instrument. See figures 7-43 and 7-44. The output stage of sampler, U14, in the microwave deck is an open-drain field-effect transistor (FET). The drain of this FET drives connector, J1, on the pc board, thus providing a current path for transistor, Q1, and forming a cascade amplifier. The bandwidth of this amplifier is nominally dc to 20 MHz.

4-220. The collector of Q1 drives transistor, Q2, which acts as a unity gain buffer. The emitter of Q2 is ac coupled through impedance-matching components R5 and C3 to drive a 3 stage passive filter. The 3 dB cutoff frequency of this filter is 20 MHz with a notch at 33.33 MHz which serves to filter out any leakage of the sampling frequency. The output of this filter drives U1, an ECL line receiver containing three amplifiers connected in series to provide approximately 45 dB gain. The output from U1 pin 14, nominally 1 MHz, drives phase detector U2.

4-221. IC, U2, compares the frequency of U1 output with a reference signal generated by U7. This signal is either 1 MHz or 333.3 kHz depending on the rf output frequency of the instrument. In the 2 to 6 GHz band, U7 pin 10 is high and U7 divides its 1 MHz input by 1. In all other bands, U7 pin 10 is low and U7 divides its input by 3. This is necessary as the output oscillator is locked via the third harmonic of the reference oscillator output.

4-222. The phase detector outputs are pulsed signals which are integrated by R9, C13, R10, and C14, before feeding amplifier U3, pin 3. The output of this amplifier passes through a notch filter centered at 1 MHz to the input of switch U6.

4-223. When the output frequency of the instrument is in the range of 0 to 18 GHz, switch U6 will feed the notch filter output to the base of Q5, which drives Q6, forming a high current gain Darlington pair. The output of Q6 drives the fm coil of the 2 to 6 GHz oscillator. At output frequencies above 18 GHz, switch U6 will feed the notch filter output to the base of Q3, which drives Q4, forming a second Darlington pair. The output of Q6 drives the fm coil of the 4 to 8.7 GHz oscillator.

4-224. IC, U3 pin 7, is present to ensure that the loop locks on the appropriate comb line are generated by the sampler. Operation of this circuit is identical to that described in the section for A11, fixed LO assembly. Comparators, U4 and U5, provide an out of lock indication. Operation of this circuit is identical to that described in the section for A11, fixed LO assembly.

4-225. A15, POWER DISPLAY PCB ASSEMBLY

4-226. This circuit provides a visible indication of either the selected output power of the instrument, in dBm, or the amplitude of an input signal applied to the built-in power meter. See figures 7-20 and 7-21. IC, U1, is an analog-to-digital converter which changes the analog voltage from level control assembly, A3, into digital form. The outputs of U1 drive the 7-segment latching LED display integrated circuits, U2 through U5. IC, U9, regulates a +15 volt supply to +5 V to provide power for U1 and to minimize the effects of high-current transients on the rest of the instrument. Zener diode, VR1, provides a precise reference voltage for U1.

4-227. The output of U1 is multiplexed bcd data representing the voltage input to the integrated circuit. Digit-select strobes appear on U1 pins 16, 17, and 18, where these are buffered by U7 to drive the latch strobes on U3 through U5. The data outputs from U1 pins 20 through 23 are buffered by U6 and drive the data inputs of the display integrated circuits. Transistors, Q1 and Q2, and dual latch, U8, decode and drive the polarity (+ −) and most-significant-digit LED display U2. Lamp test functions are implemented for all displays by the presence of a logic "low" at the lamp test input pin 4.

4-228. Two dual LED indicators, DS1 and DS2, provide visual indication of the instrument LOCK and LEVEL status. When the voltage on the LOCK or LEVEL input is approximately 0 V, the green LED is forward-biased and illuminates, while the red LED is reverse-biased and off. When the input reaches +8 V or more, the green LED is reverse-biased and off, while the red LED is forward-biased and illuminates. Pulsed signals to the two inputs may cause both LEDS to flash on alternately, appearing to produce a range of intermediate colors.

4-229. A16, FREQUENCY DISPLAY PCB ASSEMBLY

4-230. This circuit provides a visual indication of the instrument rf output frequency regardless of operating mode, and a visual indication of whether the instrument functions are being controlled from the front panel or via the IEEE 488 bus. See figures 7-22 and 7-23. ICs, U1 through U5, are latching 7-segment LED displays which are driven by the instrument internal frequency-data-distribution bus. Thus, these five displays directly display the rf output frequency at any instant, whether the unit is sweeping or operating at a fixed frequency. Transistor, Q2, is driven by the REMOTE select line and turns REMOTE display DS1 on when the instrument is being controlled by the IEEE 488 bus.

4-231. ICs, U6 and U7, decode the 10s GHz and 1s GHz information to drive Q1 collector "low", thus producing a lamp-test indication on U1 through U5. Whenever a frequency of 27 GHz or greater has been selected, this serves as an overrange indicator. Diode, CR1, decouples the lamp-test inputs of the displays from the remainder of the lamp-test line so that only the frequency display is affected under these conditions.

4-232. A17, LEVER SWITCH PCB ASSEMBLY

4-233. This assembly consists of the front-panel frequency select lever switches, the delta-F lever switches, and associated multiplexing circuitry. See figures 7-24 and 7-25. IC, U2, decodes the instrument internal data-transfer address bus to sequentially produce eight mutually exclusive outputs. The outputs of U2 drive high-current buffers, U1 and U3, which in turn raise the common input of the selected lever switch from a logic "low" to "high". The diode matrix couples the state of the switch to the four output lines. As the common inputs of all other switches are "low," only the data from the one switch is transferred. This produces a bcd number on output pins 7 through 10, which is sent to frequency control assembly, A7, for further processing. As the switches are scanned in sequence, the positions of all switches are eventually sensed.

4-234. A18, 10 MHz REFERENCE PCB ASSEMBLY

4-235. This circuit produces a low-noise, crystal-controlled 10 MHz reference signal with extremely low spurious signal components. This master reference frequency for the entire instrument, is phase locked to either the internal 10 MHz time base or to an external 1 MHz source. See figures 7-45 and 7-46.

4-236. The logic state at U2 pin 9 is controlled by the front-panel 1 MHz INT/EXT switch. This logic level determines whether the internal 10 MHz temperature compensated crystal oscillator (TCXO) or an external 1 MHz source is used as the instrument master reference frequency. When this line is low the TCXO is selected, and when high the frequency applied to the unit front panel EXTERNAL 1 MHz connector, as amplified by Q1, is selected. As the frequency of the TCXO is divided by 10 via U3, the output signal at U2 pin 11 is always 1 MHz. The output of U2 is sent to phase detector U5.

4-237. Crystal Y1, voltage variable-capacitance diode CR2 and Q2 form a VCO whose output is buffered by Q3 and Q4. The output of Q4 is sent to the 33.3 MHz reference assembly, A12, for further processing. This signal also drives divider U4 which produces a 1 MHz signal which is the second input of phase detector U5. This device compares the output of U4 to the 1 MHz reference and the relative phase information is converted by U6 to a form suitable for driving the VCO circuit, thus completing the loop.

4-238. A19, A20 SAMPLER DRIVER PCB ASSEMBLY

4-239. A19 amplifies the 33.33 MHz signal from the 33.33 MHz reference assembly, A12, to drive reference sampler, U14, which controls the frequency of the instrument reference oscillator. Assembly A20 drives down converter sampler U15 to control the frequency of the down converter oscillator when operating in the 0 to 2 GHz band. A19 and A20 are identical assemblies. See figures 7-68 and 7-69.

4-240. The 33.33 MHz input from A12 is applied at the input connector. This signal is tuned and impedance-matched by the high-selectivity tank circuit composed of C1, C2, C5, C6, C7, L1, and L2, and drives the base of Q1. The collector of Q1 is tuned by C3, C19 and L3. The amplified 33.33 MHz signal drives rf power transistor Q2 through C12 and a ferrite bead which suppresses spurious oscillations. Transistor, Q2, is a class-C output stage which is tuned by C4, C14, and L4. The inductor is tapped at the appropriate point to match the impedance of the cable connected to the output jack and the load presented by the sampler. IC, U1, provides the appropriate regulated voltage for the circuit operation and serves to minimize the effect of the high current rf signal on the remainder of the instrument.

4-241. A21, DOWN CONVERTER AND HARMONIC FILTER ASSEMBLY

4-242. This assembly amplifies the 0 to 2 GHz signal from mixer, U17, and filters out unwanted harmonics. The assembly is composed of four circuit boards, A21A1 through A21A4, located in a shielded housing. One of these pc boards contains the digital control circuits which select the appropriate filters. A second board houses the amplifier and a switching circuit. The remaining two boards mount eight low-pass filters. See figures 7-70 through 7-75.

4-243. The control circuits use PROM U1 to decode the parallel frequency data. The outputs of U1 are processed by U2 and U4 and control relay drivers U3 and U5. Some of the relay drive outputs are utilized external to the assembly to select low-pass filters in the 500-to-2000 MHz region, while the remainder, select filters internal to the assembly for the 100 to 500 MHz region.

4-244. The signal from mixer, U17, is applied to J1. If this signal is above 500 MHz it is passed by PIN diode CR2, but not passed by PIN diode CR1. The output of CR2 is applied to J2 for amplification and filtering external to the assembly. If the signal is below 500 MHz it is passed by CR1 and not passed by CR2. The output of CR1 is slightly attenuated and presented to broadband amplifier U1. The output of U1 is further amplified by U2. This signal is applied to the inputs of the two filter boards within the assembly. Depending on the selected frequency, one of these filters is selected, while the others remain out of circuit. All of these filters are fixed tuned except the 300 to 499 MHz filter, which, due to stray capacitance, requires 3 tuning adjustments.

4-245. A22, VIDEO AMPLIFIER PCB ASSEMBLY

4-246. This pc board works in conjunction with level control assembly, A3, to control the power level of the rf output. The output power of the instrument is constantly monitored using a directional coupler and diode detector. Due to the limited bandwidth of the couplers it is necessary to use two coupler/detector units, one for the 0 to 1 GHz band and the other for the 1 to 26 GHz band. See figures 7-47 through 7-49.

4-247. The outputs of these two detectors are applied to the video amplifier rather than directly to the level control board, as the signal levels are extremely low and therefore susceptible to noise degradation. Also, since the diode output impedances are quite high, pulse response of the detectors would suffer if these were required to drive significant capacitances as would occur in the cable lengths necessary to reach level control assembly, A3.

4-248. The outputs of microwave detectors U22 and U20 feed the inputs of video amplifier U4 and U3, respectively. These amplifiers have gains of nominally 40 dB nominal and very low risetimes. The latter characteristic is required when the instrument is operating in the pulsed mode. As the detector outputs are negative in polarity it is necessary to provide a fixed dc offset in order to keep the detector signals within the dynamic range of U3 and U4. Depending on the instrument output frequency, the output of U3 or U4 is selected by relay K1 and appears at J3. ICs, U3 and U4, require +/−8 V supplies which are generated locally by U1 and U2. A stable reference voltage for the required offset is provided by zener diode VR1.

4-249. A26, FET SWITCH PCB ASSEMBLY

4-250. This circuit controls the application of power supply and tuning current to the oscillators such that only the correct oscillators are energized for a given output frequency. The selection of oscillators is controlled by seven band select logic lines from oscillator driver assembly, A6. These signals appear on terminals 1, 10, 11, 12, 13, 14 and 17 and drive comparators is generated by CR1 and CR2 and is approximately 1.4 volts. See figures 7-91 and 7-92.

4-251. Assume an output frequency in the 4 to 8 GHz band. One side of the main tuning coil of this oscillator is connected to a +15 volt supply, the other side to terminal 7 on the pc board. Terminal 12 will be "high," therefore U2 pin 8 is "high." This turns on Q2 and completes a current path for the 4 to 8 GHz oscillator maintune coil from terminal 7 to terminal 8 on the pc board. This terminal is connected to the drain of transistor Q1 on the instrument chassis. The gate of Q1 is driven by oscillator driver assembly, A6, to control output oscillator tuning current.

4-252. Also, Q15 turns on thus connecting the +15 volt supply to the 4 to 8 GHz oscillator, and Q12 is turned on by U6 pin 7 to connect the −5.2 volt supply to this oscillator. A damping network formed by C5 and R15 is used to reduce the noise of the driver. Diode CR7 is necessary to reduce the very large voltage spikes generated by the inductance of the oscillator tuning coil when switched on or off. Suitable damping networks and diodes are provided for the other oscillators as well.

4-253. The remaining sections of this circuit operate in a similar manner. Table 4-2 shows which transistors are switched on as the output frequency varies.

Table 4-2. FET Switching Configuration

Frequency GHz	Output Oscillator and Transistors On	Reference Oscillator and Transistors On
0-2	8-12 Q3, Q17	2-6 Q9, Q10, Q11, Q12, (Q15)
2-4	2-4 Q1, Q16	2-6 Q9, Q10, Q11
4-6	4-8 Q2, Q15	2-6 Q9, Q10, Q11, Q12
6-8	4-8 Q2, Q15	2-6 Q9, Q10, Q11, Q12
8-12	8-12 Q3, Q17	2-6 Q9, Q10, Q11
12-18	12-18 Q4, Q5, Q14	2-6 Q9, Q10, Q11
18-26	18-26 Q6, Q7, Q13	4-8 Q8, Q12, Q15

NOTE

In the 0 to 2 GHz range the 4 to 8 GHz oscillator is locked at 8.001 GHz to mix with the 8 to 10 GHz signal from the output oscillator to produce 0 to 2 GHz. Thus, the transistors which energize the 4 to 8 GHz oscillator are also turned on.

4-254. It should be noted that the supply voltages appearing on terminals 18, 21 and 22 are used only if transistor, rather than Gunn diode, oscillators are used. If Gunn diode types are used the V_b bias supply is generated by the oscillator driver assembly, A6. Also, the 18 to 26 GHz oscillator derives its tuning current from the +20 volt supply rather than a +15 volt supply as do the other oscillators.

4-255. A27, MODULATOR PCB ASSEMBLY

4-256. There are three functions incorporated on modulator assembly, A27. These are: (1) the modulator driver circuits which provide the drive currrents for the pulse modulators; (2) a +6 volts (nominal) regulator which provides an intermediate voltage for YIG filter FL1; and, (3) a switch which turns on sampler-driver, A20, when the instrument output frequency is between 100 MHz and 2 GHz. See figures 7-93 and 7-94.

4-257. Modulator Driver Circuit

4-258. The rf modulators in Model 1626 are PIN diodes located in microwave modules U5, U8, and U11. These modules are constructed so that the diodes greatly attenuate the signal when conducting, and offer little attenuation when not conducting. Each modulator requires 5 to 20 milliamperes forward current for maximum attenuation of the rf signal, and 0.5 to 1.0 volts reverse bias for minimum attenuation. The forward current, reverse bias, and rise and fall times of these currents must all be carefully controlled in order to produce optimum modulation of the rf signal.

4-259. To compensate for propagation and switching delays in the digital, analog, and microwave circuitry, level control assembly, A3, requires 75 to 150 nanoseconds delay between start of the sample-and-hold cycle, necessary to produce proper output levels when the rf signal is being modulated, and the start of the rf output pulse.

4-260. A replica of the selected TTL modulating signal from level control assembly, A3, initiates the sample-and-hold cycle on A3. This signal is also applied to the input of the modulator driver; and thus, the two one shot multivibrators, which comprise U3, IC, U3 pin 13 is triggered on the negative edge of the signal; and U3 pin 5 on the positive edge. The outputs of these two multivibrators are pulses approximately 65 nanoseconds long.

4-261. The outputs from U3 (pin 13) and U3 (pin 5) trigger U4 (pin 4) and U4 (pin 12) on the negative edge of these pulses. IC U4 (pin 4) produces an output about 90 nanoseconds after application of the negative-going edge of the modulator driver input pulse. IC U4 (pin 12) produces and output about 90 nanoseconds after the positive-going edge of the input pulse.

4-262. IC U5 is configured as an RS flip-flop. The pulse from U4 (pin 4) sets the flip-flop, and the pulse from U4 (pin 12) resets it. Thus the signal at U5 (pin 6) is a replica of the input pulse, delayed by about 100 nanoseconds. A control line from level control assembly, A3, guarantees that the flip-flop will be in the correct state if the instrument is turned on in the CW mode.

4-263. The output from U4 (pin 12) is applied through R5 and C5 to the base of transistor, Q1, which inverts the signal and shifts its level. The output of Q1 is coupled via R7 and C6 to Q2. Diodes, CR1 and CR2, prevent Q1 and Q2 from saturating , thus decreasing the switching times. Transistors Q3, Q4, and Q5, along with associated components, are emitter followers which provide the drive currents for the PIN diode modulators. Each of these circuits is identical. For convenience only, the circuit of Q3 will be discussed

4-264. When Q2 is not conducting, the voltage divider formed by resistors, R16 and R21, places Q3 base at approximately −1.3 volts. Transistor, Q3, emitter is therefore at −2 volts. This voltage is divided by resistors, R22 and R30, to apply about −1 volt to the PIN modulator, turning it off and allowing minimum insertion loss in the modulator.

4-265. When Q2 conducts, it acts as a switch to place resistors, R9 and R15, in parallel with R16. The base and emitter of Q3 begin to go positive. When the emitter reaches +1.1 volt, the voltage at the modulator diodes is +0.55 volts and these begin to conduct, holding the voltage at the top of R30 nearly constant. The base and emitter of Q3 continue to go positive until these reach some higher voltage (e.g. +3.5 volts).

4-266. The majority of the increasing current through R22 is thus applied to the modulator diodes, turning these fully on and the rf signal off. As the current through R30 is approximately constant after the modulator diodes begin to conduct, the voltage across R22 determines the current into the modulator. This voltage is determined by the emitter voltage of Q3, which in turn, is set by resistors, R9, R15, R16, and R21. When Q2 is turned off, the base of Q3 falls again to −1.3 volts. The majority of the charge in the modulating diodes is removed through R30, the low resistance of which allows the diodes to turn off very quickly.

4-267. The inherent differences in turn on and turn off times of the modulator and associated analog and digital circuitry can be eliminated by varying the widths of the outputs from U3 (pin 13) and U3 (pin 5). Resistors, R1 and R2, allow adjustment of these widths. The rf pulse which is a replica of the TTL input pulse is delayed by approximately 100 to 150 nanoseconds. The signal at the MOD IN/OUT jack of the instrument occurs somewhat earlier than the rf pulse, thus enhancing its use as a triggering signal for the user.

4-268. Voltage Regulator Circuit

4-269. YIG filter, FL1, requires a relatively stable and noise-free tuning current in order to avoid possible amplitude modulation of the rf output in the 2 to 12 GHz band. This current is provided by the voltage output of adjustable regulator, U1. IC, U1, varies its conductivity to keep a constant voltage (approximately 1.2 volts) between pins 1 and 2 of the device.

4-270. Resistor, R13, sets the current necessary to produce this voltage drop, and thus the voltage across R12. The output voltage of the device is thus determined by these two resistors. The value of R12 is selected to produce a nominal +6 to +8 volts at the output terminal, as required by the individual YIG filter used in the instrument.

4-271. 0 to 2 GHz Switch Circuit

4-272. The function of this circuit is to turn off sampler driver assembly, A20, when it is not needed, to eliminate one possible source of spurious signals in the rf output when operating at a frequency of 2.000 GHz or above.

4-273. In the 0.1 to 1.999 GHz band, the 0 to 2 GHz logic line is at a TTL high level (+2 to +5 volts). At 2.000 GHz and above, this line is at a TTL low level (0 to +0.8 volts). When the 0 to 2 GHz line is high, the voltage at the 0 to 2 input pin is at +2.0 volts. Diode, CR3, a dual diode in a single package, has approximately 1.4 volts across it when conducting. Current flows from the logic line through CR3 and R10, to the −15 volt supply, placing the base of Q6 at approximately +0.6 volts, turning Q6 off.

4-274. The base of Q7 is connected to the collector of Q6 and to the −15 volt supply through R11. The Q7 emitter is connected to the power input of sampler driver assembly, A20. When Q6 is off, Q7 will be forward-biased through R11 and will conduct, applying current to A20, turning it on. When the 0 to 2 GHz logic line is at a TTL low, the voltage at the 0 to 2 input pin will be less than +0.8 volts, and the base of Q6 will be approximately −0.7 volts. Transistor, Q6, will conduct, bringing its collector and the base of Q7 to ground: Q7, thus, has no bias between its emitter and base, and does not conduct. This removes the −15 volt power supply from A20, turning it off.

CHAPTER 5

MAINTENANCE

5-1. INTRODUCTION

5-2. This chapter contains procedures to maintain the operating characteristics and specifications of the Model 1626 Microwave Synthesizer. A list of test equipment is included and designates the equipment required for each subsequent section.

5-3. REQUIRED TEST EQUIPMENT

5-4. Table 5-1 lists the recommended test equipment for the Model 1626 Microwave Synthesizer.

Table 5-1. Recommended Test Equipment

Type	Model	ATP	CAL	Repair
1. Frequency Counter, 26 GHz	SD 6246A	Required	Required	Required
2. Digital Voltmeter, 4-1/2 digit	SD 7362A		Required	Required
3. Spectrum Analyzer, 26 GHz	HP 8565 + Mixer	Required	Required	Required
4. Power Meter 26 GHz	HP435 + Heads	Required	Required	Required
5.Oscilloscope, 250 MHz	Tek 475A	Required	Required	Required
6. Detector, 26 GHz	Weinschel	Required	Required	Required
7. IEEE-488 Controller	SD 3522			Required

5-5. PERFORMANCE TEST

5-6. The following procedure is recommended to verify proper synthesizer operation and conformance to specifications. The tests are grouped according to the type of measurement equipment being used for verification. Allow 30 minutes warm-up prior to performance calibration procedures.

NOTE

The amplitude accuracy specification of the Model 1626 approaches and in some cases equals that of commonly available power measuring equipment. Also the VSWR of any rf adapter must be considered. For these reasons care in interpreting amplitude accuracy measurements must be exercised.

5-7. Connect the frequency counter to the UUT output.

1. Set the UUT to 10 GHz with no modulation or sweep; output amplitude at 0 dBm.
2. Verify that the output is within 10 kHz (connect counter timebase to a known standard).
3. Vary each of the 1 MHz through 1 GHz digits over the range of 0 to 9 and verify that the output follows.
4. Set the UUT first to 1 GHz, then 21 GHz, and verify proper output.
5. Disconnect the counter.

5-8. Connect the 0.1 to 18 GHz power meter to the UUT output. Observe "NOTE" stated in paragraph 5-6.

1. Set the UUT for +5 dBm out, no modulation and no sweep.
2. Vary the frequency from 0.1 to 18 GHz in 100 MHz steps and verify that the output amplitude is within ± 1 dB of +5 dBm.
3. Set the 1 dB attenuator to −9 dB.
4. Vary the frequency from 0.1 to 18 GHz in 100 MHz steps and verify that the output amplitude is within ± 1 dB of −4 dBm.
5. Return the 1 dB attenuator to 0 dB and turn the LEVEL control fully clockwise.
6. Vary the frequency from 0.1 to 18 GHz in 100 MHz steps and verify that the output amplitude equals or exceeds +5 dBm.
7. Replace the 0.1 to 18 GHz power meter with one that covers 18 to 26 GHz.
8. Repeat steps 1 through 6, varying the frequency from 18 to 26 GHz in 100 MHz steps.
9. Disconnect the power meter.

5-9. Connect the spectrum analyzer to the UUT output.

1. Set the analyzer rf attenuator to 40 dB.
2. Select 200 MHz on the UUT with no modulation or sweep, and at +5 dBm. Establish a reference level on the analyzer and set the analyzer to 20 kHz/cm.
3. Change the UUT to 100 MHz and, without changing any analyzer settings, note the amplitude of any signal at 200 MHz. It should be 55 dB or more below the reference.
4. Repeat steps 2 and 3 at 700/350 MHz.

5. Repeat steps 2 and 3 at 1000/500 MHz.
6. Repeat steps 2 and 3 at 1600/800 MHz.
7. Set the analyzer rf attenuator to 10 dB.
8. Repeat steps 2 and 3 at 5/2.5 GHz.
9. Repeat steps 2 and 3 at 10/5 GHz.
10. Repeat steps 2 and 3 at 16/8 GHz.
11. Repeat steps 2 and 3 at 24/12 GHz (use mixer).
12. Set the UUT to 185 MHz and center the signal on the analyzer with the peak at the top.
13. Vary the analyzer frequency span from 100 MHz/cm to 20 kHz/cm. Note any spurious signals (must be at least 55 dB below the carrier).
14. Repeat step 13 at 376 MHz.
15. Repeat step 13 at 3.920 GHz.
16. Repeat step 13 at 9.111 GHz.
17. Repeat step 13 at 16.666 GHz.
18. Repeat step 13 at 19.333 GHz.
19. Set the UUT for a −4 dBm output with no modulation or sweep.
20. Set the UUT to 7.0 GHz and establish a reference level on the analyzer.
21. Switch to ⎍⎍ (squarewave modulation) with the MOD P.R.F. counterclockwise to 1 kHz PRESET and the X5 pushbutton out.
22. Set the analyzer to zero span and maximum intermediate frequency (if) bandwidth. Adjust the rf/if attenuation to display an on-scale signal (use minimum rf attenuation). Adjust the sweep speed and sync to display the squarewave. Note the p-p reading; should be >30 dB.
23. Repeat steps 20 through 22 at 15 GHz.
24. Repeat steps 20 through 22 at 22 GHz.
25. Set the UUT for 0 dBm output, with no modulation and a frequency of 6 GHz.
26. Select a ΔF of 800 MHz with a 1 kHz sweep rate.
27. Verify on the analyzer that the signal is sweeping about 800 MHz, starting at 6 GHz.
28. Verify, using the oscilloscope, a ramp at the SWEEP OUT connector. It should be about 10 V p-p.
29. Verify a negative-going pulse at the rear PEN LIFT connector. The pulse width depends on the setting of the (internal) retrace time.
30. Repeat steps 27 through 29 with a .1 kHz rate.
31. Disconnect the spectrum analyzer.

5-10. Connect the detector to the UUT output.

1. Terminate the detector in 50 Ω and connect it to the oscilloscope.
2. Set the UUT for 3 GHz at +5 dBm with no sweep.
3. Select ⎍⎍ (pulse) modulation and, by varying the MOD P.R.F. control and X5 pushbutton, verify a rate of ≤100 Hz to ≥50 kHz.
4. Set the MOD P.R.F. to 1 kHz PRESET and verify a 1 kHz rate.
5. Set the MOD P.R.F. to maximum (50 kHz and vary the PULSE WIDTH control to verify 0.1 to 10 μs.
6. Select ⎍⎍ (squarewave).
7. Verify a squarewave out.
8. Monitor the MOD connector with the oscilloscope and verify a TTL level squarewave.
9. Connect the pulse generator to the MOD connector (approximately 10 kHz rate, 10 μs width) and verify proper operation with ⎍⎍, EXT ⎍, and EXT ⎍.
10. Remove the 50 Ω termination.
11. Switch MODULATION from OFF to ⎍⎍ and ⎍⎍. Verify that the negative plateau remains within ± 1 dB.
12. Disconnect the detector.

5-11. Connect a short piece of semirigid coax from the UUT RF OUT connector to the POWER METER INPUT connector.

1. Set the UUT to +5 dBm.
2. Switch to POWER METER EXT and verify +5 dBm ±1 dB.
3. Set the UUT to −5 dBm (POWER METER INT).
4. Switch to POWER METER EXT and verify −5 dBm ±1 dB.
5. Set the UUT to −15 dBm (POWER METER INT).
6. Switch to POWER METER EXT and verify −15 dBm ±2 dB.
7. Set the UUT to −25 dBm (POWER METER INT).
8. Switch to POWER METER EXT and verify −25 dBm ±2 dB.

5-12. CALIBRATION PROCEDURE

CAUTION

Before removing or inserting any PCB assembly, turn off the instrument power and allow at least 30 seconds for the power supplies to discharge, to prevent damage to the subject PCB assemblies. Use care in the removal and re-insertion of the PCB assemblies to avoid any mechanical damage.

NOTE

The following procedure should be performed in its given order. Note particularly that any readjustment of the 15 DAC adjustments on the A6 assembly will require readjustment of all the other (18) A6 assembly adjustments, as well as adjustments on the A8 assembly.

NOTE

All resistance and capacitance values called out on the schematic diagrams as RXX, CXX, or nominal are selected at test. For more information consult the factory.

NOTE

This procedure is intended as a calibration and re-alignment procedure and assumes that no faulty or out-of-tolerance components are present within the equipment.

5-13. Unless otherwise noted, the front panel controls are to be set as follows:

1 MHz REF to INT
MODE to CW
MODULATION to OFF
ATTENUATOR(s) both to 0
POWER METER to INT
LEVEL to LEVELED
MOD P.R.F. to 1 kHz PRESET
PULSE WIDTH to 10 μs
CW/START, GHz to 02.000
ΔF, GHz to 0.000

5-14. A18, 10 MHz REFERENCE

1. Monitor the output of 10 MHz TCXO A18U1 at A18U3, pin 5, with a frequency counter slaved to a reference standard.
2. Verify that the frequency is between 9.999990 and 10.000010 MHz. If not, adjust the trimmer on top of A18U1 to standardize the TCXO.
3. Monitor the test point connected to A18U6, pin 6, with a DVM and adjust trimmer capacitor A18C13 for a reading of +4 to +5 V dc.

5-15. A12, 33.33 MHz REFERENCE

1. Monitor the test point on top of A12 assembly and adjust trimmer capacitor A12C19 for a reading of +4 to +5 V dc.
2. Monitor the test point with an oscilloscope and adjust BALANCE potentiometer A12R20 for a minimum duration pulse.

5-16. A19 and A20 SAMPLER DRIVERS

1. Connect an oscilloscope to pad 4 of A19 (A20) (accesible through hole in the can cover).
2. Set front panel CW/START, GHz switches to 01.000 GHz.
3. Adjust trimmer capacitors C3 and C4 for maximum peak-to-peak signal on the oscilloscope ($\cong$5 V p-p).
4. Repeat steps 1 through 3 for Sampler Driver A20.

5-17. A6 OSCILLATOR DRIVER, A13 OUTPUT PLL, AND A14 REFERENCE PLL

1. Connect a DVM to A6TP1 then verify and adjust the DAC, if necessary, in accordance with table 5-2.

Table 5-2. DAC Verification and Adjustment

Step	Front Panel CW/START, GHz Setting	DVM Reading A6TP1	Adjustment
1	02.000	+0.500 V	D/A OFFSET A6R52
2	20.000	+5.000 V	20 GHz A6R51
3	Repeat steps 1 and 2, as required.		
4	09.000	+2.250 V	D/A GAIN A5R50
5	Repeat steps 2 and 4 as compromise for minimum deviations from specified DVM readings.		

2. To verify and adjust the oscillator tracking, perform the steps in table 5-3. If the DVM reading at the indicated test point deviates from 0 volts by more than $\pm$0.0005 V, adjust the appropriate potentiometer.

Table 5-3. Oscillator Tracking Verification and Adjustment

Step	Front Panel CW/START, GHz Setting	Test Point	Adjustment Potentiometer
1	02.000	A6TP3	A6R61
2	06.000	A6TP3	A6R60
3	18.000	A6TP3	A6R59
4	02.000	A6TP2	A6R58
5	04.000	A6TP2	A6R57
6	08.000	A6TP2	A6R56
7	12.000	A6TP2	A6R55
8	18.000	A6TP2	A6R54
9	24.000	A6TP2	A6R53

3. Connect the DVM to test point A6TP2, set front panel CW/START, GHz switches to 17.000 and verify a DVM reading of −1.2500 V. If the DVM reading deviates more than ±0.5 mV, adjust OUTPUT OFFSET GAIN potentiometer A6R62 to correct.
4. Connect the DVM to test point A6TP3, set front panel CW/START, GHz switches to 11.000 and verify a DVM reading of −1.2500 V. If DVM reading deviates more than ±0.5 mV, adjust REFERENCE OFFSET GAIN potentiometer A6R63 to correct.
5. Connect the DVM to test point A14TP1. Disconnect the 50-ohm termination from U14 Reference PLL Sampler and connect a frequency counter to the SMA connector via a low-loss cable. Verify that the DVM reading is between +5.5 V to +6.0 V and frequency measured on the counter is in accordance with table 5-4 for each measurement step. If measurements deviate from table 5-4, adjust the appropriate potentiometer on the A6 assembly.

NOTE

It may be necessary to insert a small SMA pad to ensure that the counter does not lock onto a sideband due to frequency and power level changes.

Table 5-4. Reference Oscillator Setting, Verification, and Adjustment

Step	Front Panel CW/START, GHz Setting	Counter Frequency Measurement	Adjustment Potentiometer
1	02.000	1.901 GHz	A6R73
2	05.900	5.801 GHz	A6R82
3	06.000	1.967 GHz	A6R72
4	17.900	5.933 GHz	A6R81
5	18.000	5.967 GHz	A6R71
6	26.000	8.633 GHz	A6R80

6. Disconnect the frequency counter and DVM. Replace the 50-ohm termination that was removed from U14 Reference PLL Sampler.
7. Connect a frequency counter to the front panel RF OUT SMA connector and a DVM to A13TP1 (Output PLL PCB), then verify that the DVM reading is between +5.5 V to +6.0 V and the frequency counter reading is identical to the front panel setting for each step in table 5-5. If measurements deviate from table 5-5, adjust the appropriate potentiometer on the A6 assembly.

NOTE

If the YIG filter adjustments are out of limits, it may be required when performing step 7 to measure the frequency in the 2 to 12 GHz range at the output port of the 2 to 12 GHz Module U5 instead of the front panel RF OUT SMA connector.

Table 5-5. Output Tracking Verification and Adjustment

Step	Front Panel CW/START, GHz Setting	Adjustment Potentiometer
1	02.000	A6R70
2	03.000	A6R79
3	04.000	A6R69
4	07.900	A6R78
5	08.000	A6R68
6	11.900	A6R77
7	12.000	A6R67
8	17.900	A6R76
9	18.000	A6R66
10	23.900	A6R75
11	24.000	A6R65
12	26.000	A6R74

5-18. A10, OUTPUT DIVIDE-BY-N

1. Connect the oscilloscope to test point A10TP1.
2. Adjust BAL potentiometer A10R32 for minimum amplitude 1 MHz spikes.

5-19. A11, FIXED LOCAL OSCILLATOR PLL

1. Connect a DVM to A11TP1.
2. Connect a frequency counter to the front panel RF OUT SMA connector.
3. Set the front panel CW/START, GHz switches to 01.000.
4. Adjust FREQ potentiometer A11R38 for a DVM reading of +5.5 V to +6.0 V and verify a frequency counter reading of 1.000 GHz.

5-20. A9, YIG FILTER/FM DRIVER

1. Disconnect the SMB connector from A22J2 (Video Amplifier assembly).
2. Connect a power meter to the front panel RF OUT SMA connector.
3. Connect a DVM to test point A9TP1.

4. Set the front panel CW/START, GHz switches to 02.000.
5. Adjust OFFSET potentiometer A9R19 for maximum power output as indicated on the power meter, then rotate A9R19 counterclockwise for a decrease of 3 dB in output power and note the reading on the DVM. Readjust A9R19 for maximum power output as indicated on the power meter, then rotate A9R19 clockwise for a decrease of 3 dB in output power and note the reading on the DVM.
6. Readjust A9R19 to provide a DVM reading that is mid-way between the two voltage readings noted in step 5.
7. Set the front panel CW/START, GHz switches to 11.900.
8. Adjust GAIN potentiometer A9R13 for maximum power output as indicated on power meter, then rotate A9R13 counter clockwise for a decrease of 3 dB in output power and note the reading on the DVM. Readjust A9R13 for maximum power output as indicated on the power meter, then rotate A9R19 clockwise for a decrease of 3 dB in output power and note the reading on the DVM.
9. Readjust A9R13 to provide a DVM reading that is mid-way between the two voltage readings noted in step 8.
10. Repeat steps 4 through 9, as necessary.

5-21. A3, LEVEL CONTROL

1. Place the synthesizer in an environmental chamber to ensure an ambient temperature of 25°C ±2°C and power up.
2. Connect a DVM to test point A3TP4.
3. Adjust TEMP potentiometer A3R27 for a 0.00 V ±10 mV reading on the DVM.
4. Turn off power and wait at least 30 seconds.
5. Remove PROM A3U6 from its socket and jumper A3XU6 socket, pins 9 through 17, together to simulate a binary 00 PROM output.
6. Power up the synthesizer and set the front panel −10 dB STEP ATTENUATION to 0 and the LEVEL control to its LEVELED detent.
7. Connect a DVM to test point A3TP1 and adjust OS potentiomenter A3R9 for a +2.560 V ±1 mV reading of the DVM.
8. Power down the synthesizer and wait at least 30 seconds, then reconfigure the jumpers on PROM socket A3XU6 to simulate a binary FF PROM output by jumpering pins 9, 10, 11, 13, 14, 15, 16, 17 and 24 together.
9. Power up the synthesizer and adjust CORR potentiometer A3R7 for a +7.630 V ±1 mV reading on the DVM.
10. Repeat steps 5 through 9, as necessary.
11. Power down the synthesizer and wait at least 30 seconds, then remove the jumpering from A3XU6 that simulated PROM output and reinstall PROM U6 into its socket.
12. Power up the synthesizer and place the front panel POWER METER toggle switch to INT and the front panel ATTENUATION −1 dB STEP control to 0.
13. Connect a DVM to test point A3TP2 and measure and record the DVM reading.
14. Place the front panel ATTENUATION −1 dB STEP control to 9, then adjust 1 dB potentiometer A3R10 to provide a DVM reading that is 9.000 V ±1 mV greater than measured in step 13.
15. Connect the DVM to test point A3TP3 and place the front panel ATTENUATION −10 dB STEP control to 0, then measure and record the DVM reading.
16. Place the front panel ATTENUATION −10 dB STEP control to 90, then adjust 10 dB potentiometer A3R13 to provide a DVM reading that is 9.000 V ±1 mV greater than measured in step 15.
17. Set the front panel ATTENUATION STEP controls to provide 0 dB attenuation.
18. Adjust DISP OS potentiometer A3R14 for a +05.0 readout on the front panel POWER METER, dBm display.
19. Set the front panel ATTENUATION STEP controls to provide 90 dB attenuation.
20. Adjust DISP CAL potentiometer A3R15 for a −85.0 readout on the front panel POWER METER, dBm display.
21. Repeat steps 17 through 20, as necessary.
22. Connect a power meter to the front panel RF OUT SMA connector.
23. Set the front panel CW/START, GHz switches to 04.000 and the ATTENUATION STEP controls to 0 dB attenuation.
24. Adjust 1-26 CAL potentiometer A3R34 for a power meter reading of +5 dBm ±0 dBm.
25. Set the front panel ATTENUATION STEP controls to provide 9 dB attenuation, then adjust 1-26 OS potentiometer A3R36 for a power meter reading of −4 dBm ±0 dBm.
26. Repeat steps 23 through 25, as necessary.
27. Set the front panel CW/START, GHz switches to 00.500 and the ATTENUATION STEP controls to provide 0 dB attenuation, then adjust 0-1 CAL potentiometer A3R33 for a power meter reading of +5 dBm ±0 dBm.

28. Set the front panel ATTENUATION STEP controls to provide 9 dBm attenuation, then adjust 0-1 OS potentiometer A3R37 for a power meter reading of −4 dBm ±0 dBm.
29. Repeat steps 27 and 28, as necessary.
30. Connect an oscilloscope via a 26 GHz detector to the front panel RF OUT SMA connector.
31. Perform the pulse calibration steps 30 through 39 according to table 5-6.

Table 5-6. Pulse Calibration

Front Panel CW/START, GHz Setting	PCAL Adjustment Potentiometer	POS Adjustment Potentiometer
04.000	A3R21	A3R24
16.000	A3R22	A3R25
22.00	A3R23	A3R26

32. Set the front panel −1 dB STEP control to 0. Measure and note the dc level on the oscilloscope for the table 5-6 04.000 CW/START, GHz setting.
33. Set the front panel −1 dBm STEP control to 9. Measure and note the dc level on the oscilloscope for the table 5-6 04.000 CW/START, GHz setting.
34. Set the front panel MODULATION control to its CAL ⎍⎍ position, the −1 dB STEP control to 0, with the CW/START, GHz switches still in the 04.000 setting. Then, measure the level of the negative-going portion of the signal on the oscilloscope.
35. Adjust the appropriate PCAL potentiometer (refer to table 5-6) to the same level as measured in step 32.
36. Set the front panel −1 dB STEP control to 9 and measure the negative-going portion of the signal on the oscilloscope.
37. Adjust the appropriate POS potentiometer (refer to table 5-6) to the same level as measured in step 33.
38. Repeat steps 32 through 37, as necessary.
39. Repeat steps 31 through 38 for the 16 GHz and 22 GHz settings according to table 5-6.
40. Set the front panel CW/START, GHz switches to 04.000 and the MODULATION control to OFF.
41. Set the front panel −1 dB STEP control to 0. Measure and note the dc level on the oscilloscope.
42. Set the front panel MODULATION control ⎍⎍ and the PULSE WIDTH μSEC control to .1 (fully counterclockwise).
43. Measure the level of the negative-going portion of the signal on the oscilloscope. Then, adjust SAMP potentiometer A3R44 to achieve the same level as measured in step 41.
44. Repeat steps 31 through 43, as necessary.

5-22. A8, POWER METER

NOTE

The A3, Level Control pcb calibration procedure must be completed before performing the following procedure since the output of the synthesizer is used as the source to set the power meter.

NOTE

When an rf power level is called out in the following procedure, the requirement is for a measured power level accurate to ±0.1 dBm. Use a calibrated power meter (HP 435 or equivalent) to verify the power level at the end of the semirigid coax cable. Set the calibration factor of the power meter as appropriate for the frequency and power lead used. Always zero power meter before each measurement.

NOTE

When connecting a DVM to the test points called out in the following procedure always do so through an external 10 kΩ series resistor.

NOTE

Connection of the ground (Lo) probe of the DVM should be made to the ground plane of the A8 pcb.

1. Connect a DVM to test point A8TP1.
2. Set the POWER METER toggle switch to EXT.
3. Disconnect any connections or input to the POWER METER INPUT SMA connector.
4. Adjust −30 dB potentiometer A8R12 for a DVM reading of 0.0000 ±5 μV.

5. Connect a short semirigid coax cable from the RF OUT SMA Connector to the POWER METER INPUT SMA connector and set the synthesizer to 04.000 GHz.
6. Adjust the synthesizer output power level for a DVM reading of +0.200 ±1 mV.
7. Connect the DVM to test point A8TP2 and adjust the BIAS potentiometer A8R19 for a DVM reading of 0.000 V ±1 mV.
8. Connect the DVM to test point A8TP1 and adjust the synthesizer output power level for a DVM reading of 1.000 V ±5 mV.
9. Connect the DVM to test point A8TP2 and adjust SCALE potentiometer A8R21 for a DVM reading of −3.5000 V ±5 mV.
10. Apply a 0.0 dB rf power level to the POWER METER INPUT SMA connector and adjust DET GAIN potentiometer A8R5 for a DVM reading of −3.000 V ±1 mV.
11. Connect the DVM to test point A8TP3 and adjust 0 dB potentiometer A8R40 for a DVM reading of 0.000 V ±1 mV.
12. Verify that the POWER METER display reads 0.0 dBm.
13. Apply −30.0 dBm rf power level and adjust −30 dB potentiometer for a DVM reading at test point A8TP3 of −0.300 V ±1 mV.
14. Verify that the POWER METER display reads −30.0 dBm ±0.1 dBm.

NOTE

If the 0.01 to 26 GHz Detector U103 is replaced the following steps (15 through 26) should be performed to insure proper power meter calibration.

15. From the incoming 0.01 to 26 GHz Detector data sheet identify and note "F1" and "F2" which correspond to the frequencies at which the lowest (F1) and highest (F2) detector output voltages (absolute) occur.
16. Apply a +5.0 dBm rf level at a frequency corresponding to "F1".
17. Connect the DVM to test point A8TP3 and note the voltage reading. Denote this reading as V1.
18. Apply a +5.0 dBm rf level at a frequency corresponding to F2 and note the voltage reading at test point A8TP3. Denote this reading as V2.
19. Calculate V′, where V′=0.05 + (V2−V1)/2.
20. Adjust DET GAIN potentiometer A8R5 to provide a DVM reading at test point A8TP3 corresponding to V′.
21. Apply a −30.0 dBm rf level at a frequency corresponding to F1 and note the voltage reading at test point A8TP3. Denote this voltage readng as V1.
22. Apply a −30.0 dBm rf level at a frequency corresponding to F2 and note the voltage reading at test point A8TP3. Denote this voltage reading as V2.
23. Calculate V″, where V″= −0.300 + (V2−V1)/2.
24. Adjust −30 dB potentiometer A8R12 to provide a DVM reading at test point A8TP3 that corresponds to V″.
25. Apply a +10.0 dBm rf level at a frequency of 04.000 GHz and verify a POWER METER display of +10.0 dBm ±0.7 dB.
26. Perform the power meter verification for the following frequencies using table 5-7:
    - 01.000 GHz
    - 10.000 GHz
    - 20.000 GHz
    - 24.000 GHz
    - 26.000 GHz

Table 5-7. Power Meter Verification

RF Level dBm	Specified Tolerance dB
+ 5.0	±0.7
0.0	±0.7
−10.0	±0.7
−20.0	±1.3
−30.0	±1.6

CHAPTER 7

DRAWINGS

7-1. INTRODUCTION

7-2. This chapter contains the final assembly and schematic drawings for the Model 1626-01 Microwave Synthesizer. The parts list contained in chapter 6 relates to the reference designation call-outs on the diagrams. Table 7-1 provides a list by figure number of the drawings, with title, drawing number and manual page number.

Table 7-1. List of Drawings

Figure No.	Drawing Title	Drawing No.	Page No.
7-1	Microwave Signal and Control Diagram	7-075809	7-5
7-2	Function and Control Diagram	7-075809	7-6
7-3	Power Distribution Diagram	7-075809	7-7
7-4	Shipping Assembly	07591301	7-9
7-5	A1, Test Assembly – Top View (Sheet 1 of 2)	07575101	7-10
7-5	A1, Test Assembly – Bottom View (Sheet 2 of 2)	07575101	7-11
7-6	A1A1, Power Supply Heat Sink Assembly	06717302	7-12
7-7	Power Supply Schematic	7-06717302	7-13
7-8	A1A2, IEEE 488 PCB Assembly	07572502	7-14
7-9	A1A2, IEEE 488 PCB Schematic	7-07572502	7-15
7-10	A1A3, Level Control PCB Assembly	07569501	7-16
7-11	A1A3, Level Control PCB Schematic (Sheet 1 of 3)	7-07569501	7-17
7-11	A1A3, Level Control PCB Schematic (Sheet 2 of 3)	7-07569501	7-18
7-11	A1A3, Level Control PCB Schematic (Sheet 3 of 3)	7-07569501	7-19
7-12	A1A3A1 thru A1A3A3; Component Moduel Assembly	07576201 07576301 07576401	7-20
	A1A3A5 thru A1A3A7, Component Module Assembly	07576601 07576701 07576801	7-20
	A1A3A10, A1A3A11, A1A3A13 Component Module Assembly	07577101 07577201 07577401	7-20
7-12A	A1A3J1, Component Module Assembly	07576901	7-20
7-13	A1A3A4, Component Module Assembly	07576501	7-21
7-14	A1A3A9, Component Module Assembly	07577001	7-21
7-15	A1A3A12, Component Module Assembly	07577301	7-22
7-16	A1A4, Sweep Control PCB Assembly	07572701	7-24
7-17	A1A4, Sweep Control PCB Schematic (Sheet 1 of 2)	7-07572701	7-23
7-17	A1A4, Sweep Control PCB Schematic (Sheet 2 of 2)	7-07572701	7-25
7-18	A1A5, Front Subpanel Assembly	06768701	7-27
7-19	A1A5A23, Pushbutton Switch PCB Assembly	06783501	7-27

Table 7-1. List of Drawings (Cont'd)

Figure No.	Drawing Title	Drawing No.	Page No.
.7-20	A1A5A15, Power Display PCB Assembly	06726801	7-28
7-21	A1A5A15, Power Display PCB Schematic	7-06726801	7-29
7-22	A1A5A16, Frequency Display PCB Assembly	06726701	7-30
7-23	A1A5A16, Frequency Display PCB Schematic	7-06726701	7-31
7-24	A1A5A17, Lever Switch PCB Assembly	06729401	7-32
7-25	A1A5A17, Lever Switch PCB Schematic	7-06729401	7-33
7-26	A1A6, Oscillator Driver PCB Assembly	07559601	7-34
7-27	A1A6, Oscillator Driver PCB Schematic (Sheet 1 of 4)	7-07559601	7-35
7-27	A1A6, Oscillator Driver PCB Schematic (Sheet 2 of 4)	7-07559601	7-36
7-27	A1A6, Oscillator Driver PCB Schematic (Sheet 3 of 4)	7-07559601	7-37
7-27	A1A6, Oscillator Driver PCB Schematic (Sheet 4 of 4)	7-07559601	7-38
7-28	A1A6A1, A1A6A2, A1A6J1 thru A1A6J3; Component Module Assemblies	07564201 07564401 07564501	7-39
7-29	A1A7, Frequency Control PCB Assembly	06796501	7-40
7-30	A1A7, Frequency Control PCB Schematic	7-06796501	7-41
7-31	A1A8, Power Meter PCB Assembly	07575201	7-42
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7-33	A1A9, YIG Filter/FM Driver PCB Assembly	07558901	7-44
7-34	A1A9, YIG Filter/FM Driver PCB Schematic	7-07558901	7-45
7-35	A1A10, Output Divide-By-N PCB Assembly	06730101	7-46
7-36	A1A10, Output Divide-By-N PCB Schematic	7-06730101	7-47
7-37	A1A11, Fixed Local Oscillator PCB Assembly	07560901	7-48
7-38	A1A11, Fixed Local Oscillator PCB Schematic	7-07560901	7-49
7-39	A1A12, 33.33 MHz Reference PCB Assembly	06732401	7-50
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7-41	A1A13, Output PLL PCB Assembly	07538701	7-52
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7-43	A1A14, Reference PLL PCB Assembly	07561601	7-54
7-44	A1A14, Reference PLL PCB Schematic	7-07561601	7-55
7-45	A1A18, 10 MHz Reference PCB Assembly	06733201	7-56
7-46	A1A18, 10 MHz Reference PCB Schematic	7-06733201	7-57
7-47	A1A22, Video Amplifier Assembly	06777302	7-58
7-48	A1A22A1, Video Amplifier PCB Assembly	07570901	7-58
7-49	A1A22A1, Video Amplifier PCB Schematic	7-07570901	7-59
7-50	A1A24, Rear Panel Assembly	075691	7-61
7-51	A1A26, Chassis Mechanical Assembly (Sheet 1 of 2)	07569801	7-62
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7-52	A1A25A1, Microwave Chassis Assembly (Sheet 1 of 3)	07583801	7-64
7-52	A1A25A1, Microwave Chassis Assembly (Sheet 2 of 3)	07583801	7-65
7-52	A1A25A1, Microwave Chassis Assembly (Sheet 3 of 3)	07583801	7-66
7-53	A1A25A1A3, Switch Bracket Assembly	06735002	7-67
7-54	A1A25A1A5, Output Relay Bracket Assembly	06764302	7-67

Table 7-1. List of Drawings (Cont'd)

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7-57	A1A25A1A9, YIG Filter Base Assembly	07581701	7-69
7-58	A1A25A1A10, 2 to 4 GHz Bracket Assembly	06779002	7-69
7-59	A1A25A1A10A1, 2 to 4 GHz Oscillator Kit	077192	7-70
7-60	A1A25A1A11, Isolator Bracket Assembly	07581301	7-71
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7-62	A1A25A1A13, 1.9 to 6 GHz Bracket Assembly	07516202	7-73
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7-64	A1A25A1A14, Relay & Module Mounting Bracket Assembly	07580401	7-75
7-65	A1A25A1A15, Microwave Chassis Cabling Assembly	075191	7-76
7-65	A1A25A1A15, Microwave Chassis Cabling Assembly	075191	7-77
7-65	A1A25A1A15, Microwave Chassis Cabling Assembly	075191	7-78
7-66	A1A25A1A16, 4 to 8.7 GHz Y2 Oscillator Kit	077171	7-79
7-67	A1A25A1A19 & A1A25A1A20, Sampler Driver Assembly	067711	7-80
7-68	A1A25A1A19A1 & A1A25A1A20A1, Sampler Driver PCB Assembly	06767301	7-80
7-69	A1A25A1A19A1 & A1A25A1A20A1, Sampler Driver PCB Schematic	7-06767301	7-81
7-70	A1A25A1A21, Down Converter & Harmonic Filter Assembly	067583	7-82
7-71	A1A25A1A21, Down Converter & Harmonic Filter Schematic	7-067583	7-83
7-72	A1A25A1A21A1, Filter Control PCB Assembly	06752201	7-84
7-73	A1A25A1A21A2, Filter Driver PCB Assembly	06752101	7-84
7-74	A1A25A1A21A3, Filter PCB Assembly	06752001	7-85
7-75	A1A25A1A21A4, Filter PCB Assembly	06752002	7-85
7-76	A1A25A3, Terminal Board PCB Assembly	06725702	7-86
7-77	A1A25A4A, 12 to 18 GHz Y5 Oscillator Kit	077194	7-87
7-78	A1A25A4B & A1A25A5B, Oscillator Installations Assembly	075928	7-88
7-79	A1A25A4B-A1, Y5 Avantek Subassembly Oscillator (Alternate) Assembly	07593301	7-88
7-80	A1A25A4B-A1A1, 12 to 18 GHz Oscillator Kit	077195	7-89
7-81	A1A25A5A, 8 to 12 & 18 to 26 GHz Oscillator Installation Assy.	06764402	7-90
7-82	A1A25A5A-A1, 8 to 12 GHz Y4 Oscillator Kit	077196	7-91
7-83	A1A25A5A-A2 & A1A25A5B-A2A1, 18 to 26 GHz Osc. Kit	077197	7-92
7-84	A1A25A5B-A1, 8 to 12 GHz Oscillator Assembly	075934	7-93
7-85	A1A25A5B-A1A1, 8 to 12 GHz Oscillator Kit	077198	7-94
7-86	A1A25A5B-A2, 18 to 26 GHz Oscillator Assembly	075932	7-95
7-87	A1A25A6A-A1, Attenuator Bracket Assembly	06719602	7-96
7-88	A1A25A6A-A2, Coupler Bracket Assembly	07535902	7-97
7-89	A1A25A6B-A1, Attenuator Bracket Assembly	06719603	7-98
7-90	A1A25A6B-A2, Coupler Bracket Assembly	07535903	7-99

Table 7-1. List of Drawings (Cont'd)

Figure No.	Drawing Title	Drawing No.	Page No.
7-91	A1A26, Oscillator FET Switch PCB Assembly	07578101	7-100
7-92	A1A26, Oscillator FET Switch PCB Schematic	7-07577101	7-101
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7-95	A1A29, Printed Circuit Board Cover Assembly	06754492	7-104
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7-97	A3 and A4, Extender PCB Assembly	06738301	7-106
7-98	A1A28, Test Assembly Wiring (Sheet 1 of 6)	075192	7-107
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7-98	A1A28, Test Assembly Wiring (Sheet 4 of 6)	075192	7-110
7-98	A1A28, Test Assembly Wiring (Sheet 5 of 6)	075192	7-111
7-98	A1A28, Test Assembly Wiring (Sheet 6 of 6)	075192	7-112

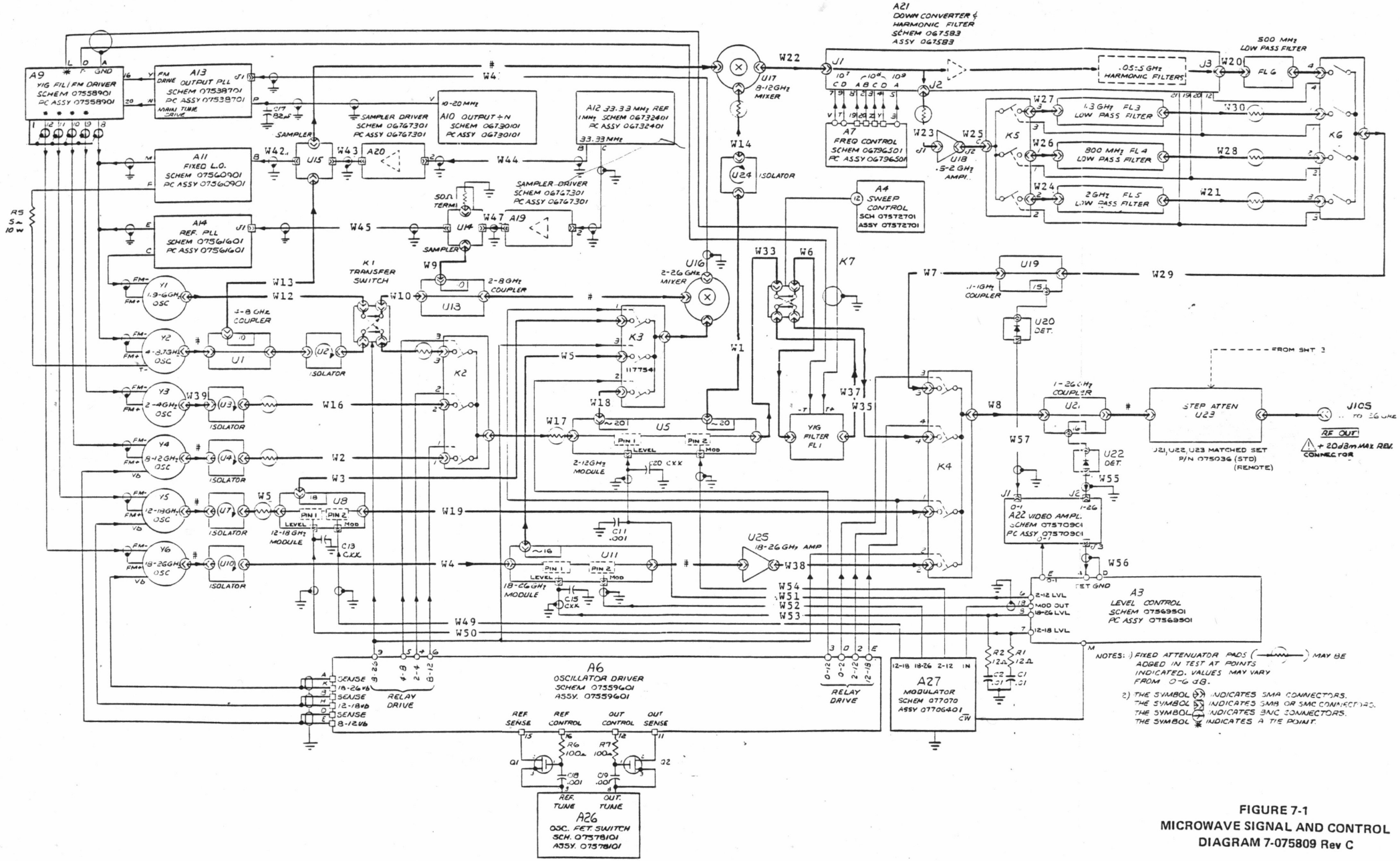


FIGURE 7-1
MICROWAVE SIGNAL AND CONTROL
DIAGRAM 7-075809 Rev C

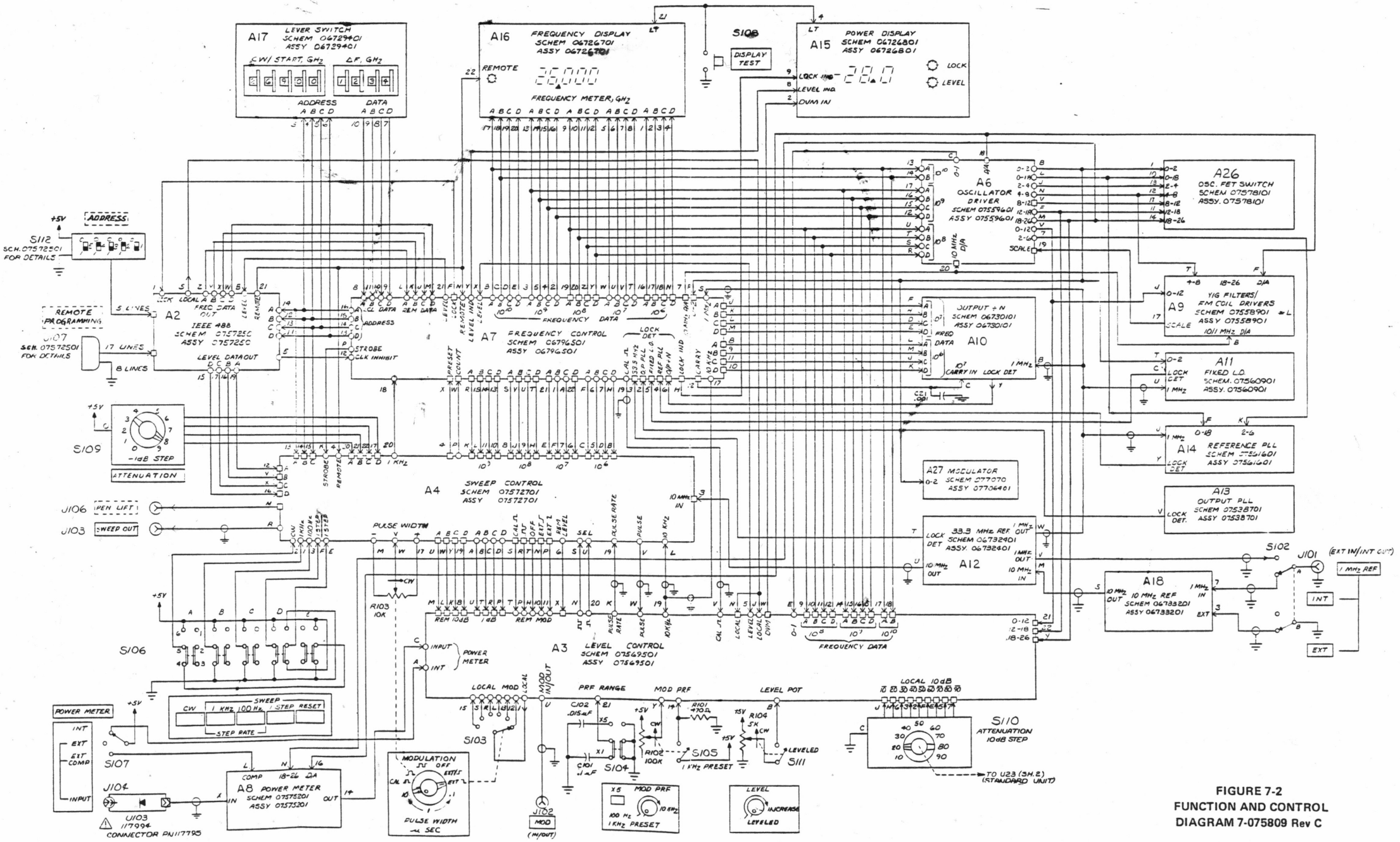


FIGURE 7-2
FUNCTION AND CONTROL
DIAGRAM 7-075809 Rev C

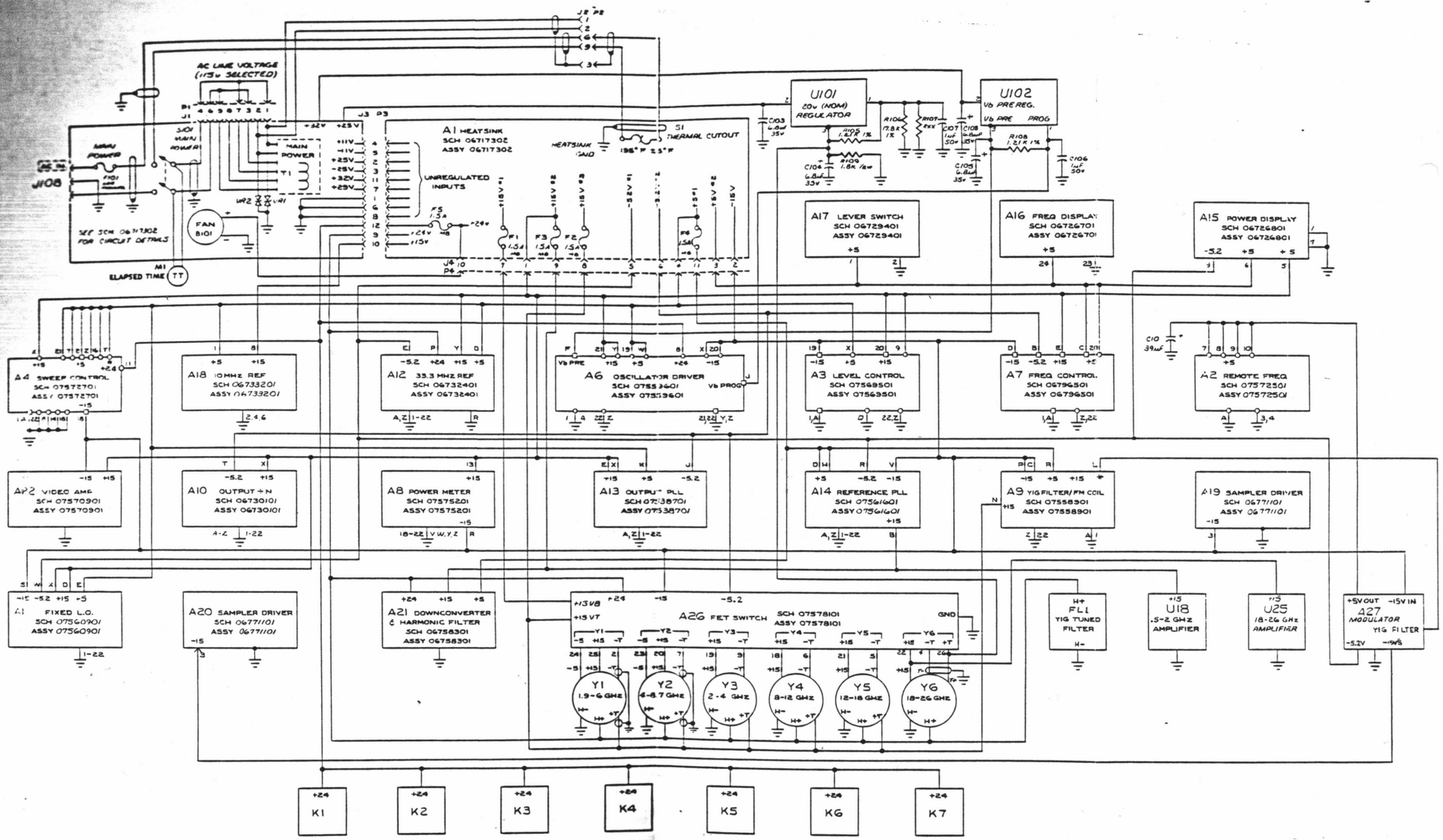
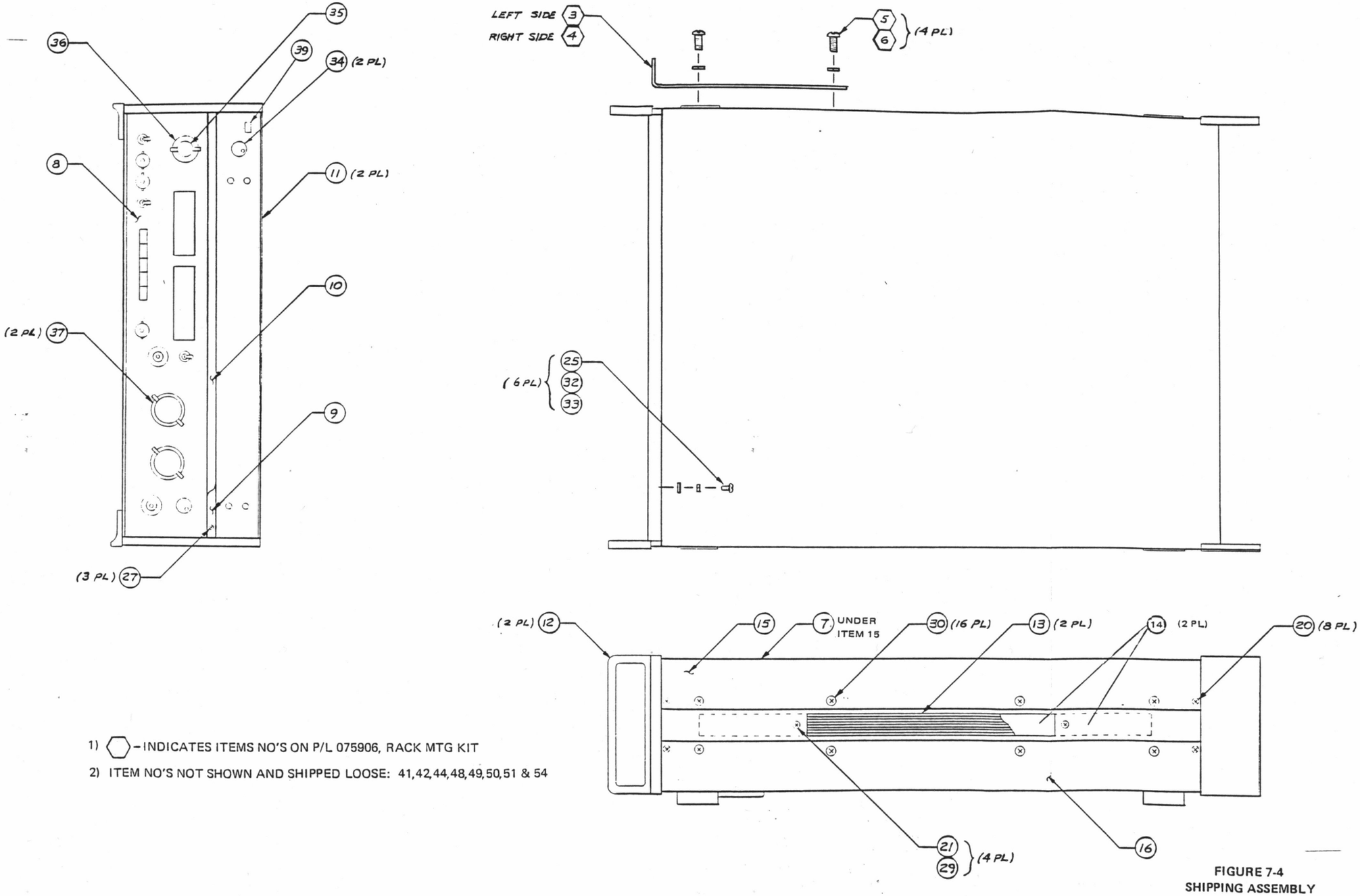


FIGURE 7-3
POWER DISTRIBUTION
DIAGRAM 7-075809 Rev C



1) ⬡ – INDICATES ITEMS NO'S ON P/L 075906, RACK MTG KIT

2) ITEM NO'S NOT SHOWN AND SHIPPED LOOSE: 41,42,44,48,49,50,51 & 54

FIGURE 7-4
SHIPPING ASSEMBLY
07591301 Rev A

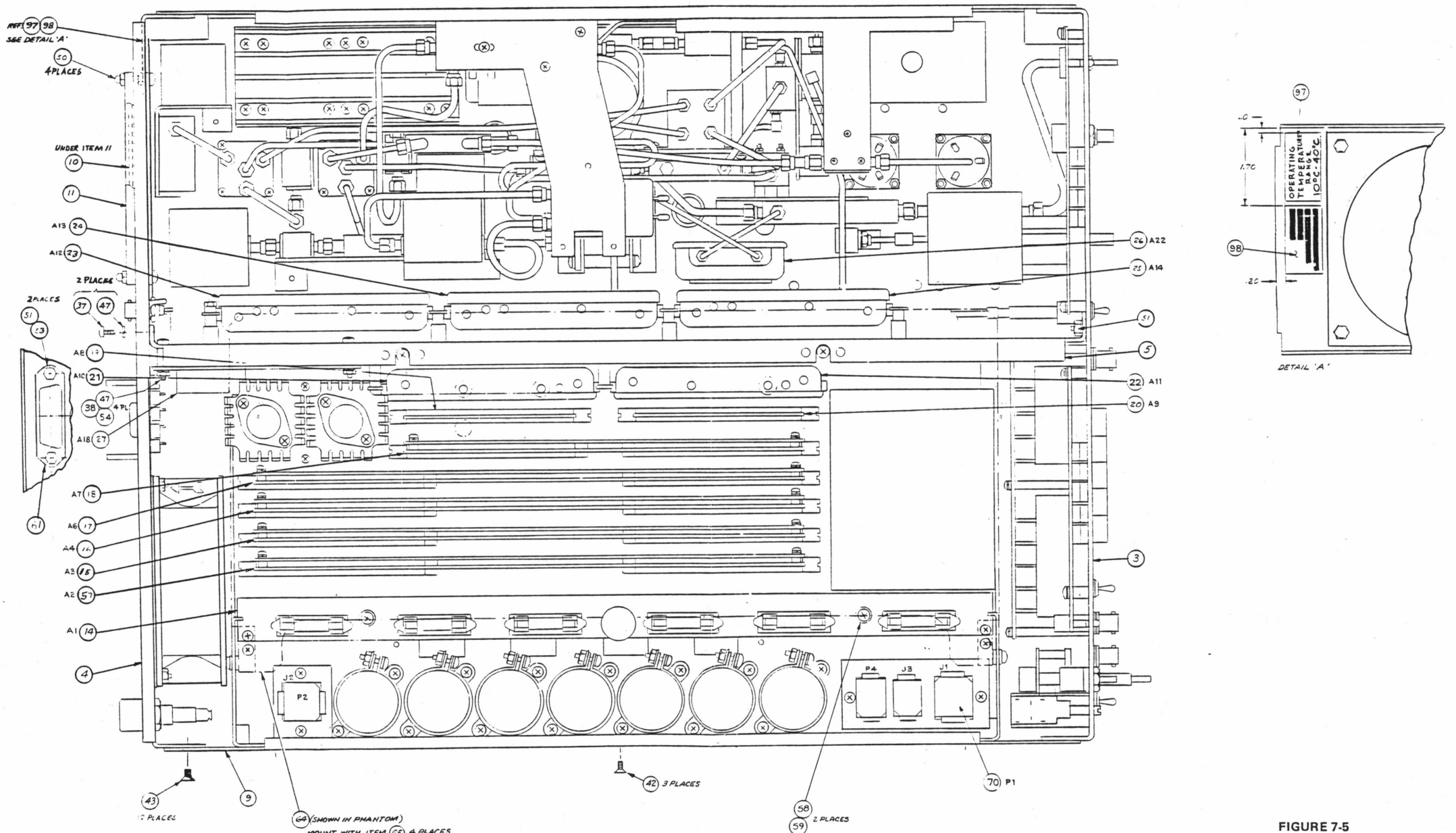


FIGURE 7-5
A1, TEST ASSEMBLY (TOP VIEW)
07575101 Rev E (Sheet 1 of 2)

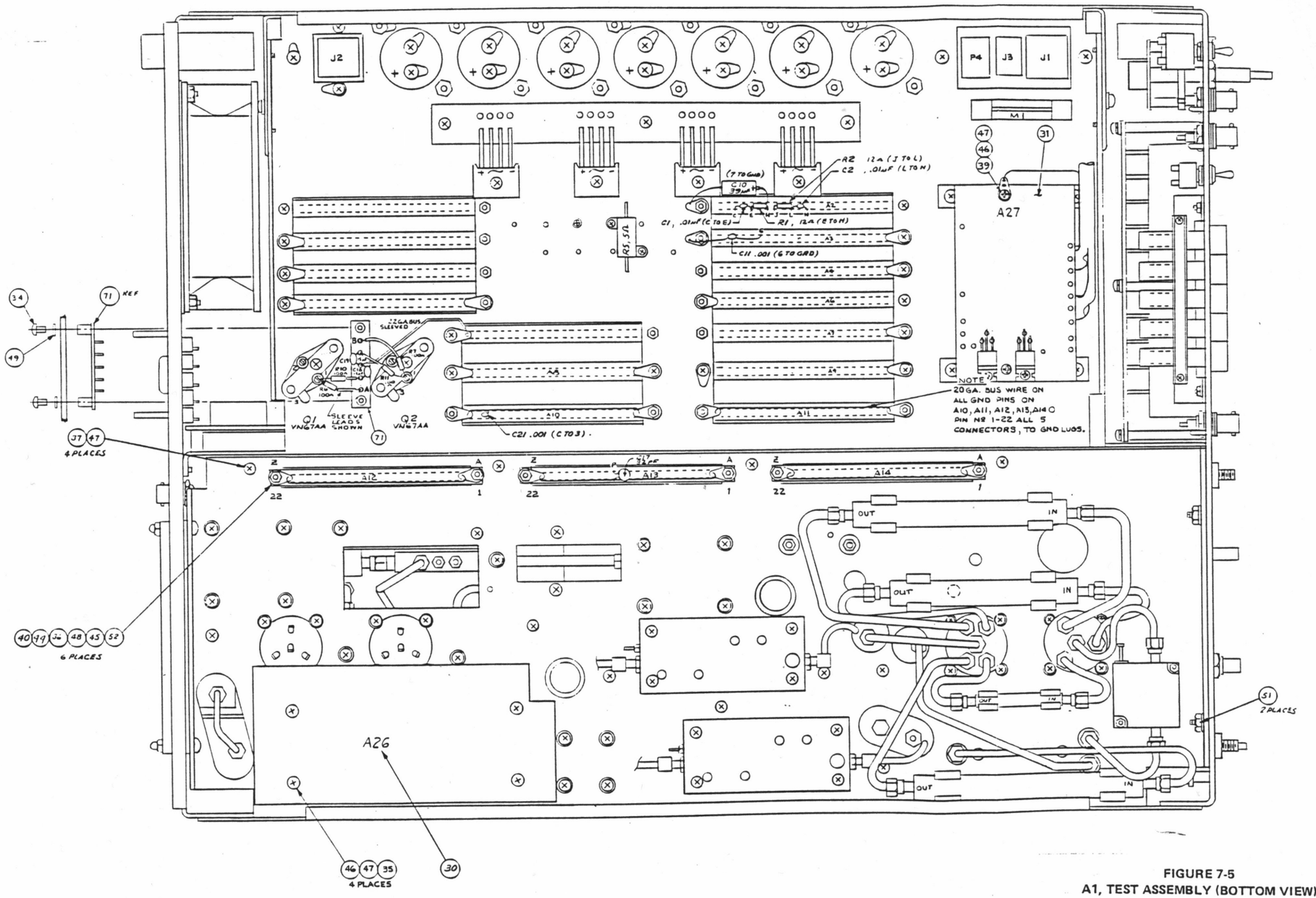


FIGURE 7-5
A1, TEST ASSEMBLY (BOTTOM VIEW)
07575101 Rev E (Sheet 2 of 2)

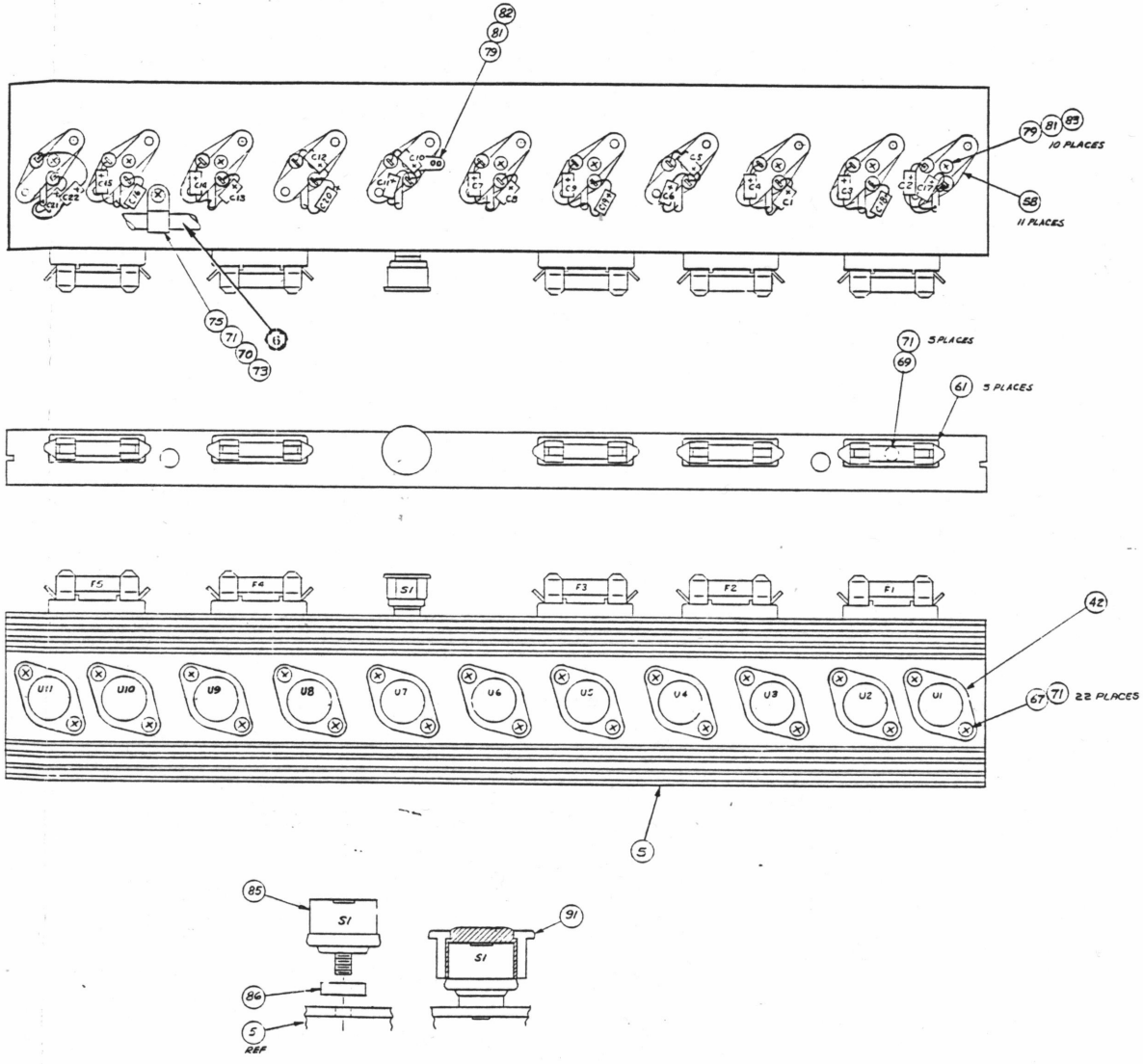


FIGURE 7-6
A1A1, POWER SUPPLY HEAT SINK
ASSEMBLY 06717302 Rev A

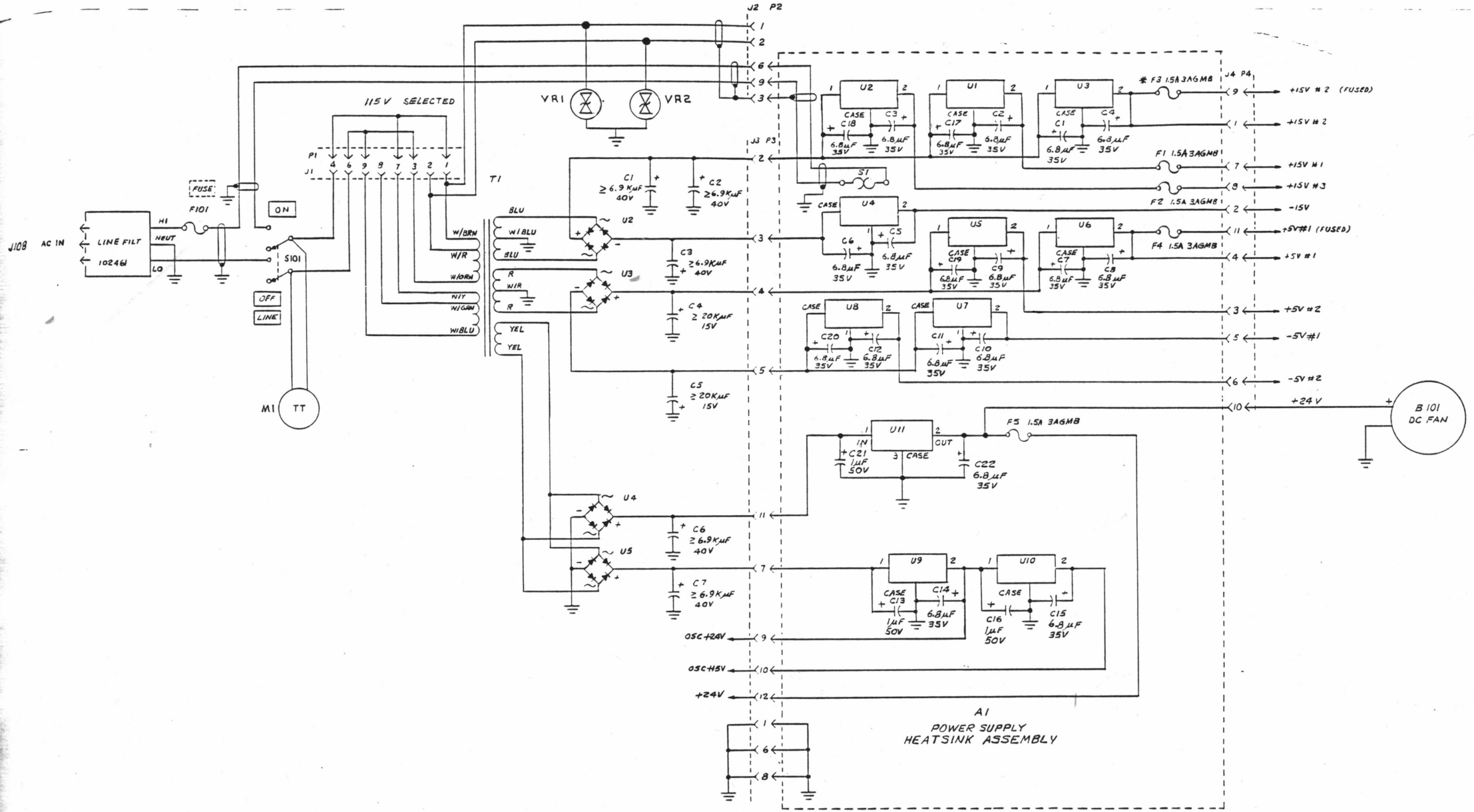


FIGURE 7-7
POWER SUPPLY (INCLUDING A1A1)
SCHEMATIC 7-06717302 Rev A

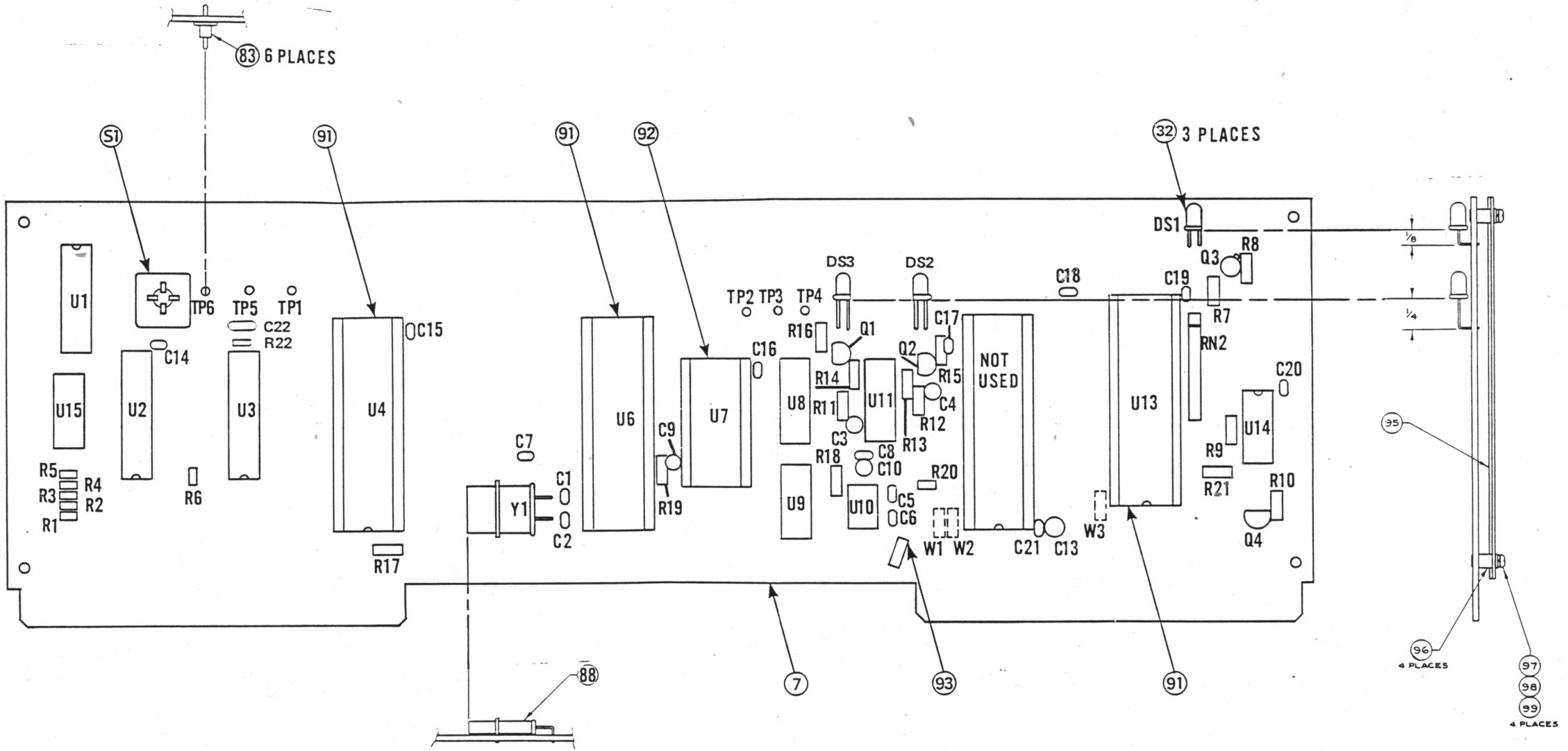


FIGURE 7-8
A1A2, IEEE 488 PCB ASSEMBLY
07572502 Rev D

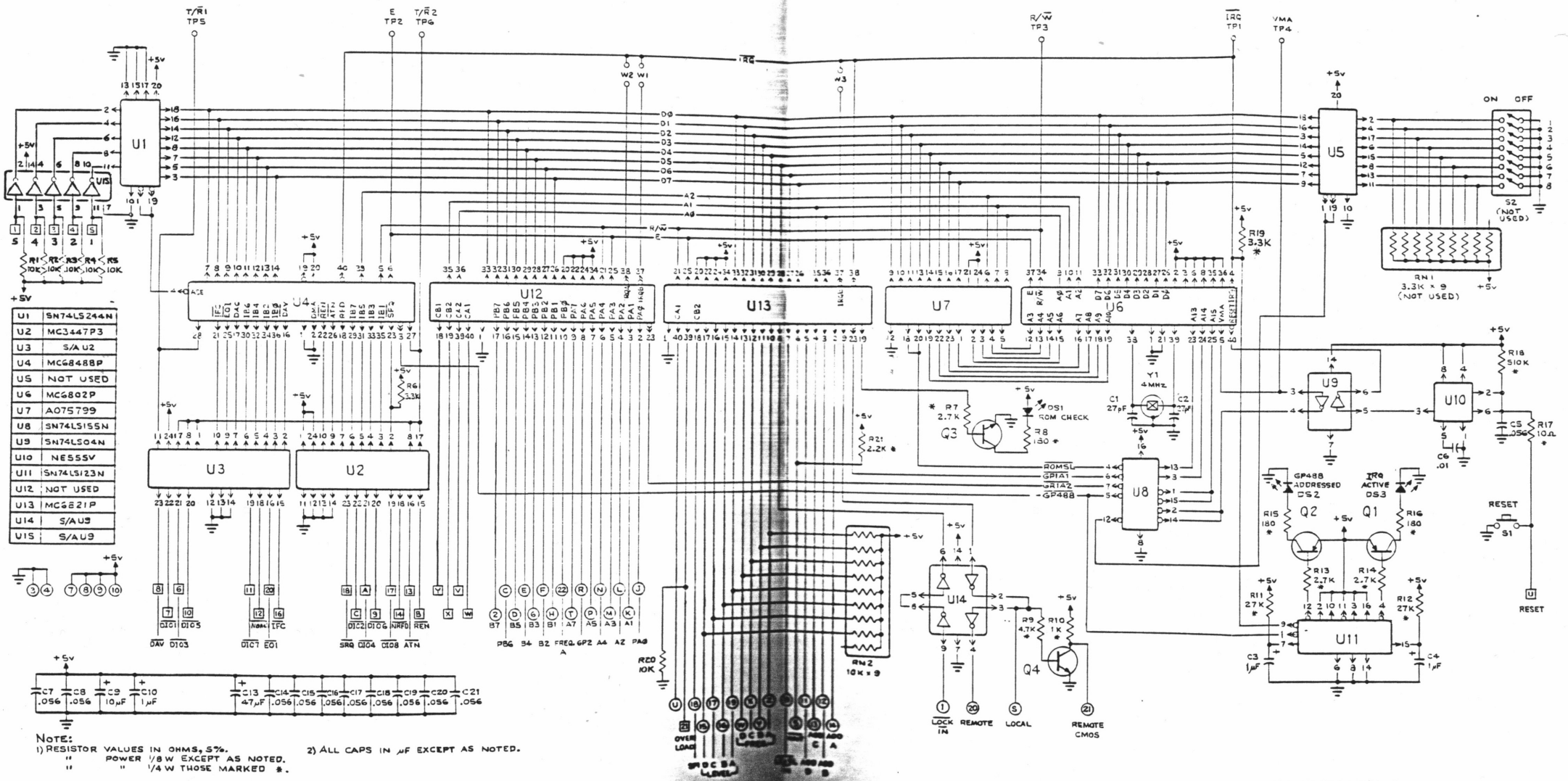


FIGURE 7-9
A1A2, IEEE 488 PCB SCHEMATIC
7-07572502 Rev C

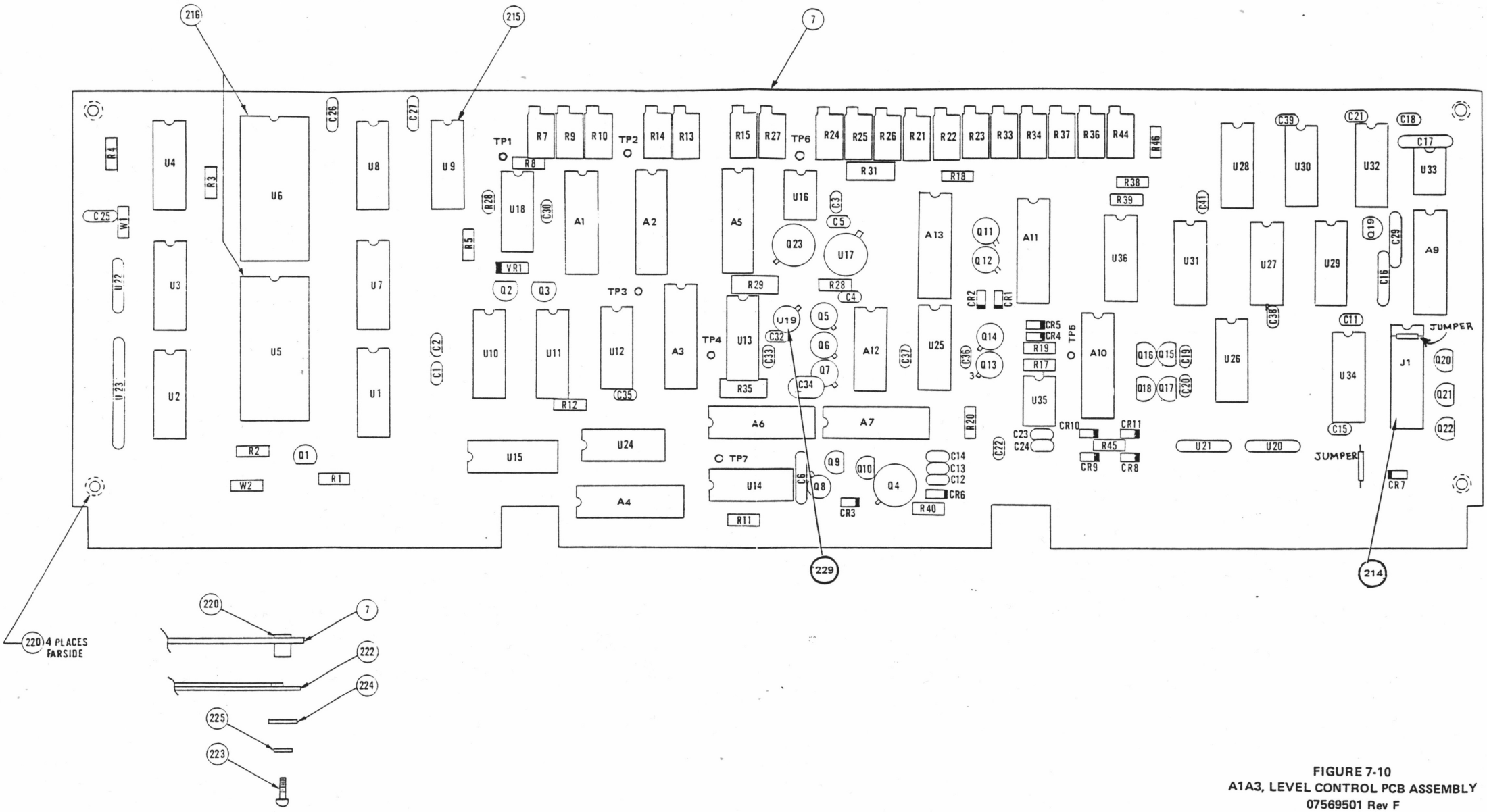
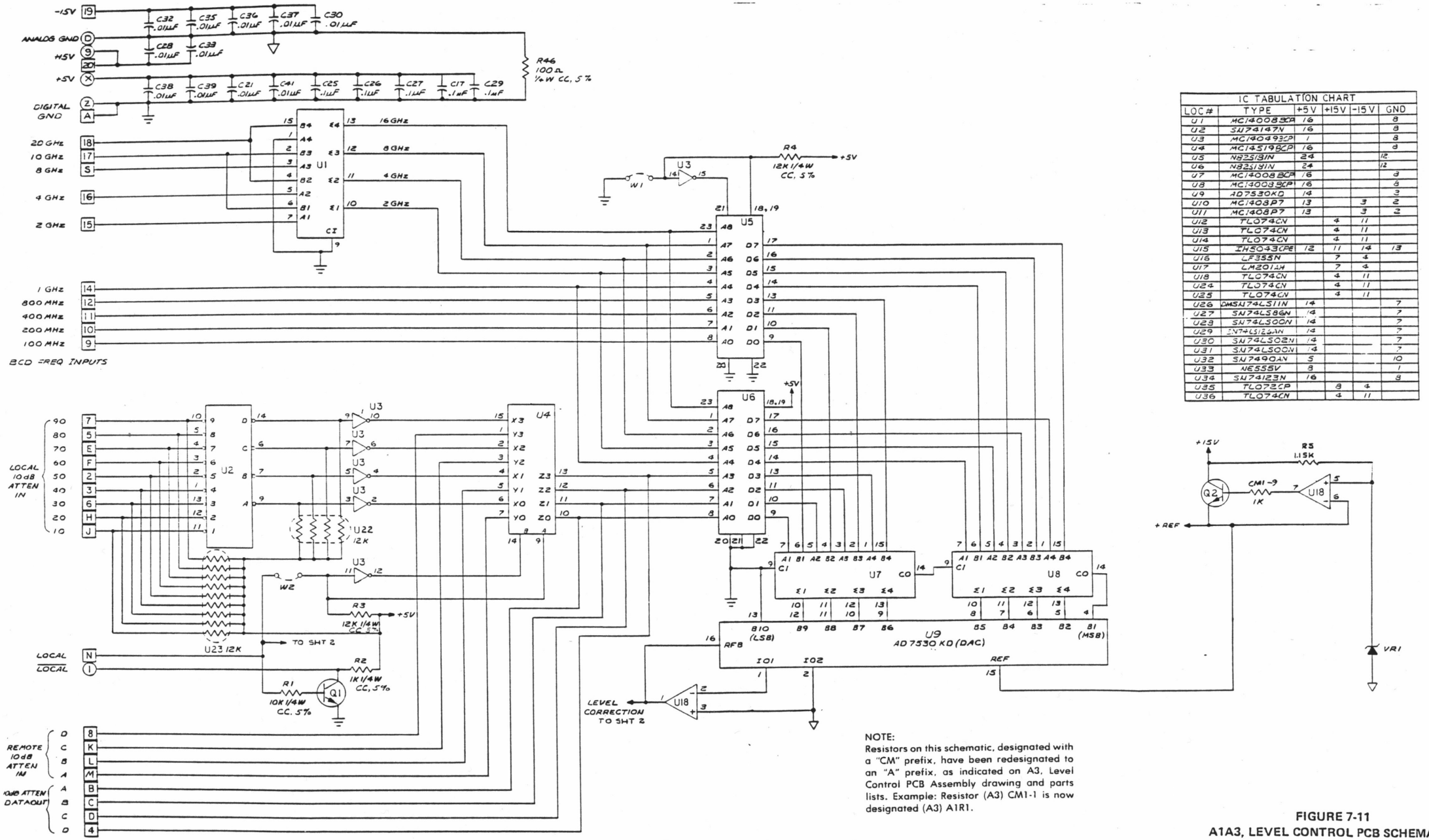


FIGURE 7-10
A1A3, LEVEL CONTROL PCB ASSEMBLY
07569501 Rev F

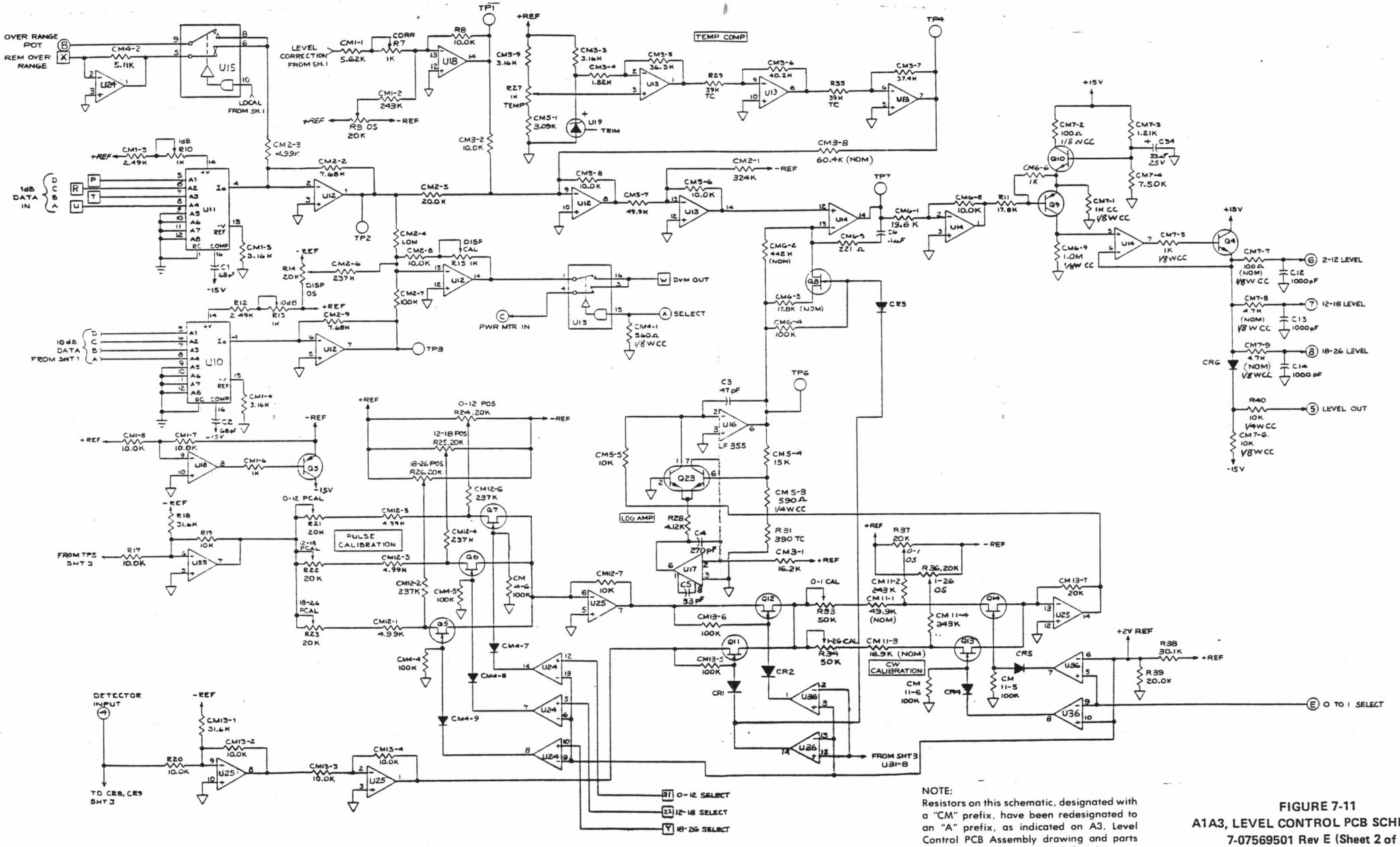


IC TABULATION CHART					
LOC #	TYPE	+5V	+15V	-15V	GND
U1	MC14008BCP	16			8
U2	SN74147N	16			8
U3	MC14049BCP	1			8
U4	MC14519BCP	16			8
U5	N8251BIN	24			12
U6	N8251BIN	24			12
U7	MC14008BCP	16			8
U8	MC14008BCP	16			8
U9	AD7530KD	14			3
U10	MC1408P7	13		3	2
U11	MC1408P7	13		3	2
U12	TL074CN		4	11	
U13	TL074CN		4	11	
U14	TL074CN		4	11	
U15	IH5043CPE	12	11	14	13
U16	LF355N		7	4	
U17	LM201AH		7	4	
U18	TL074CN		4	11	
U24	TL074CN		4	11	
U25	TL074CN		4	11	
U26	DMSN74LS11N	14			7
U27	SN74LS86N	14			7
U28	SN74LS00N	14			7
U29	SN74LS126AN	14			7
U30	SN74LS02N	14			7
U31	SN74LS00N	14			7
U32	SN7490AN	5			10
U33	NE555V	8			1
U34	SN74123N	16			8
U35	TL072CP		8	4	
U36	TL074CN		4	11	

NOTE:
Resistors on this schematic, designated with a "CM" prefix, have been redesignated to an "A" prefix, as indicated on A3, Level Control PCB Assembly drawing and parts lists. Example: Resistor (A3) CM1-1 is now designated (A3) A1R1.

FIGURE 7-11
A1A3, LEVEL CONTROL PCB SCHEMATIC
7-07569501 Rev E (Sheet 1 of 3)

"CAL" SETS ABS. POWER



NOTE:
Resistors on this schematic, designated with a "CM" prefix, have been redesignated to an "A" prefix, as indicated on A3, Level Control PCB Assembly drawing and parts lists. Example: Resistor (A3) CM1-1 is now designated (A3) A1R1.

FIGURE 7-11
A1A3, LEVEL CONTROL PCB SCHEMATIC
7-07569501 Rev E (Sheet 2 of 3)

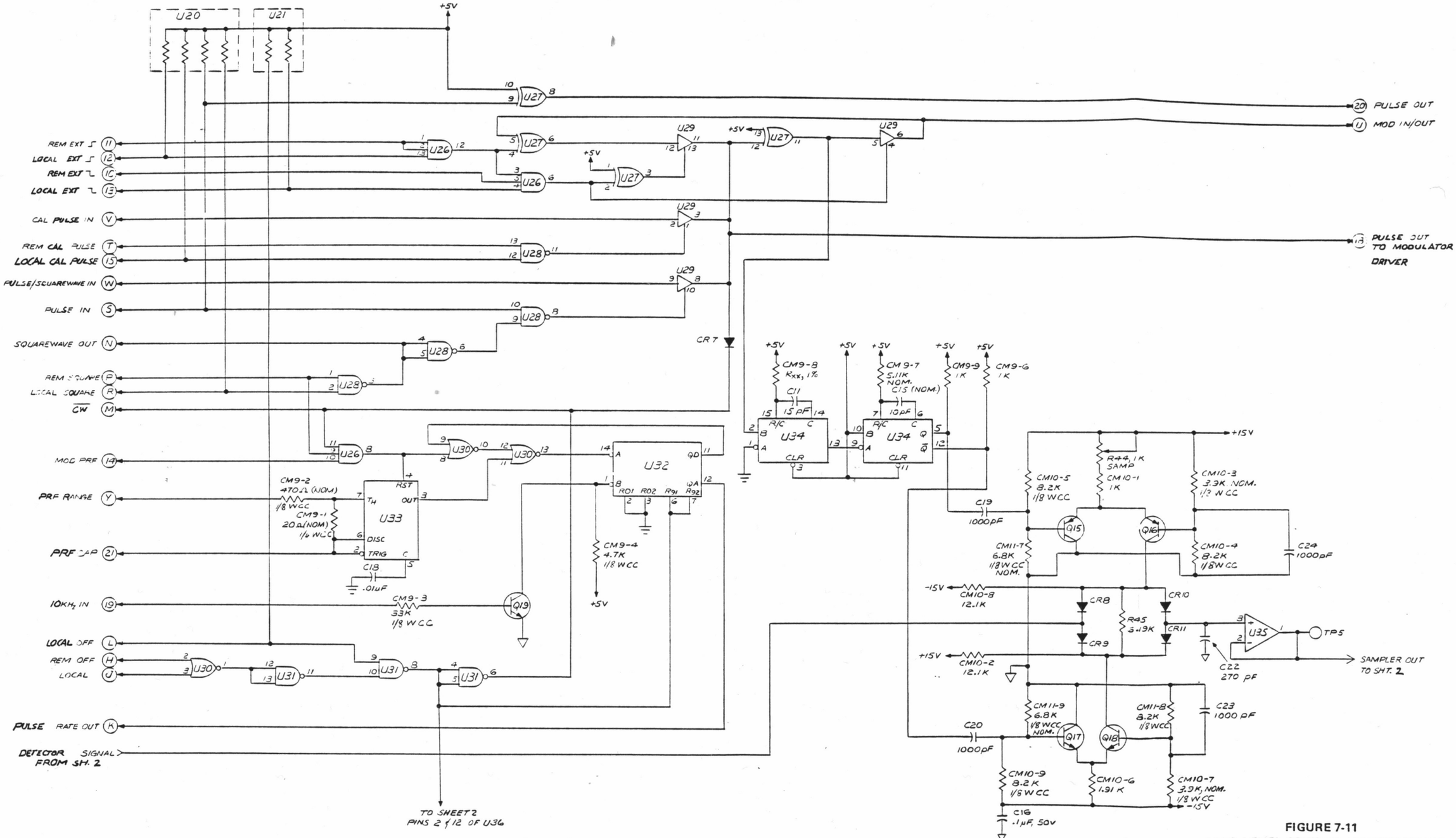


FIGURE 7-11
A1A3, LEVEL CONTROL PCB SCHEMATIC
7-07569501 Rev E (Sheet 3 of 3)

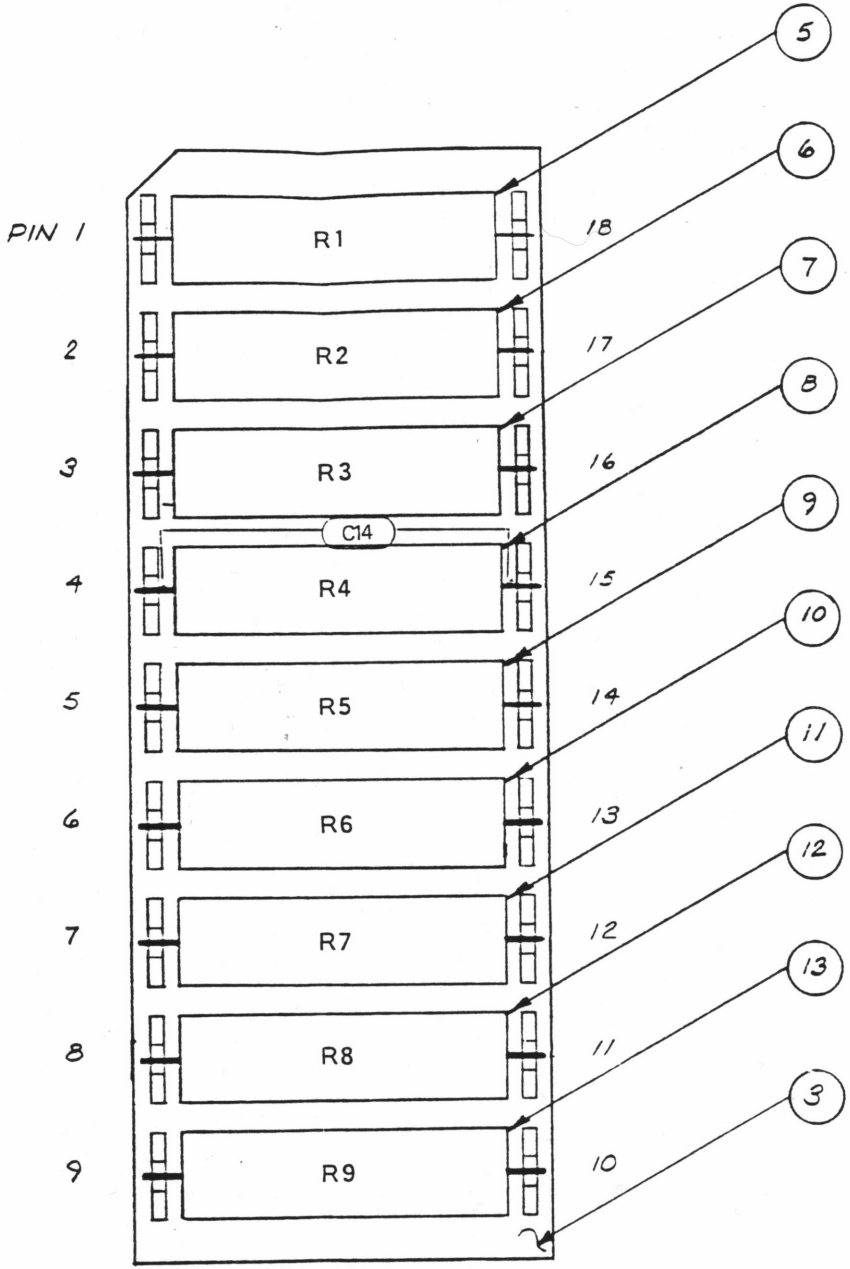


FIGURE 7-12
A1A3A1 thru A1A3A3, COMPONENT MODULES
ASSEMBLIES 07576201 Rev A, 07576301 Rev C, 07576401 Rev B;
A1A3A5 thru A1A3A7, COMPONENT MODULES
ASSEMBLIES 07576601 Rev B, 07576701 Rev B, 07576801 Rev C;
A1A3A10, A1A3A11, A1A3A13, COMPONENT MODULES
ASSEMBLIES 07577101 Rev B, 07577201 Rev A, 07577401 Rev A

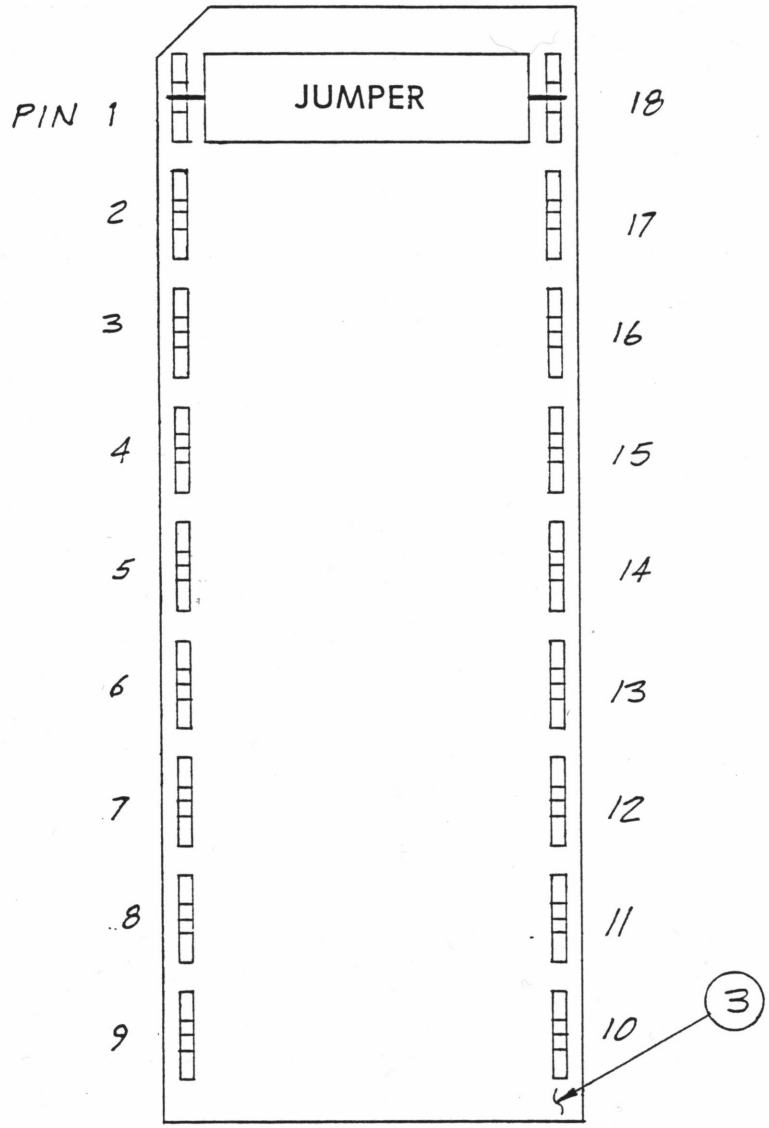


FIGURE 7-12A
A1A3J1, COMPONENT MODULE ASSEMBLY
07576901 Rev B

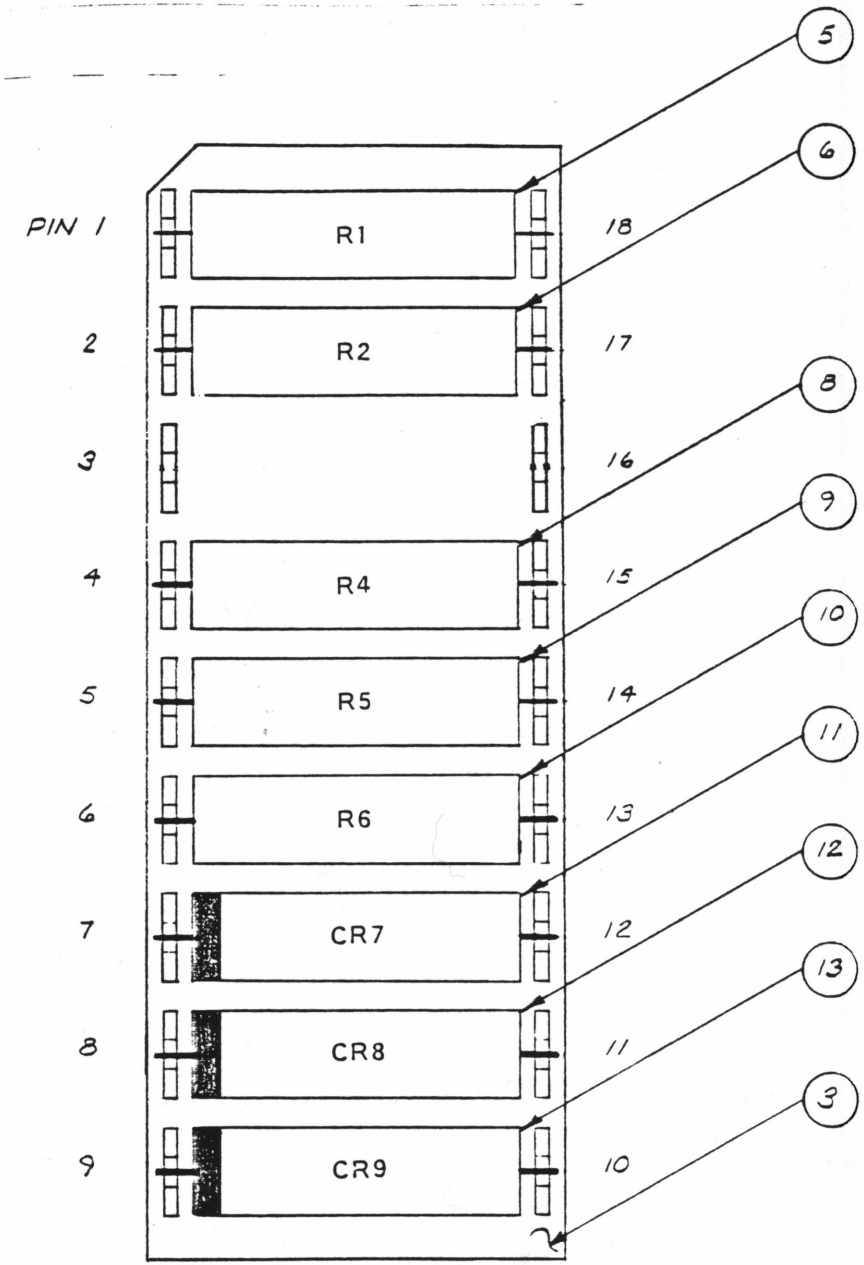


FIGURE 7-13
A1A3A4, COMPONENT MODULE ASSEMBLY
07576501 Rev B

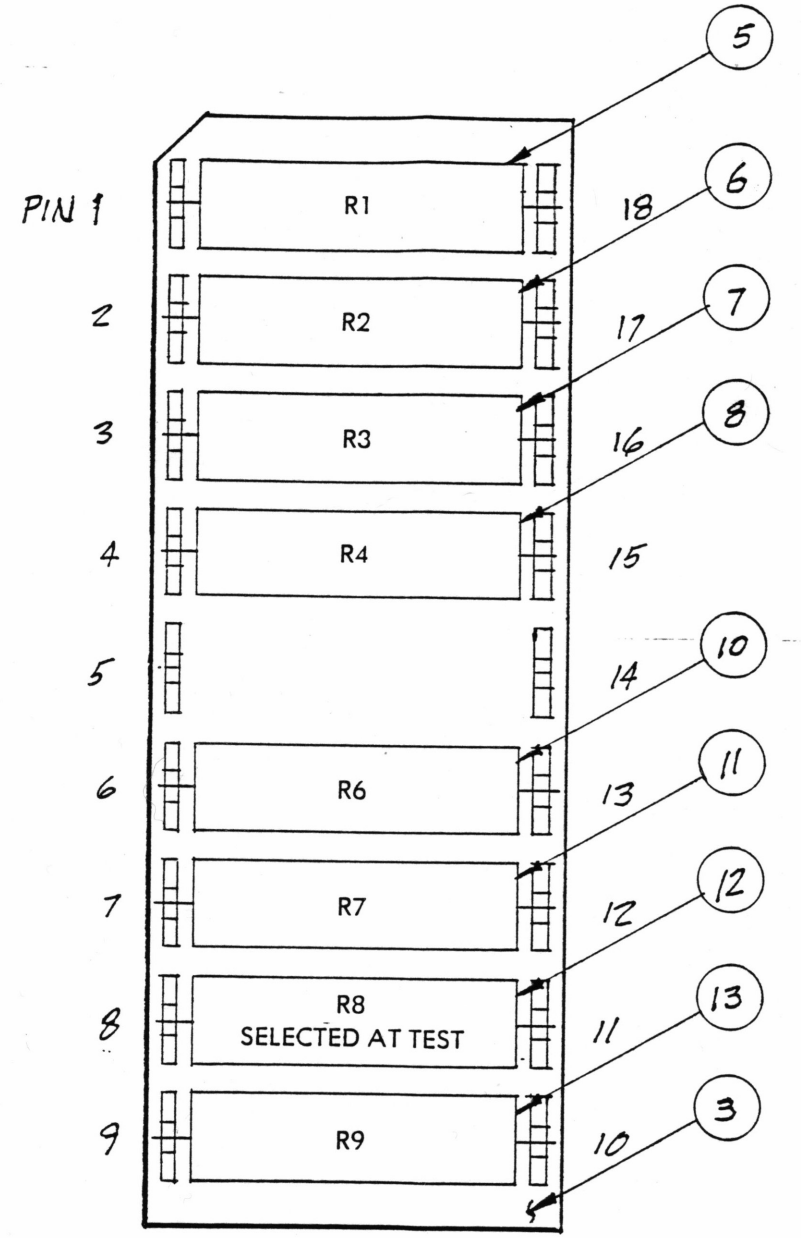


FIGURE 7-14
A1A3A9, COMPONENT MODULE ASSEMBLY
07577001 Rev D

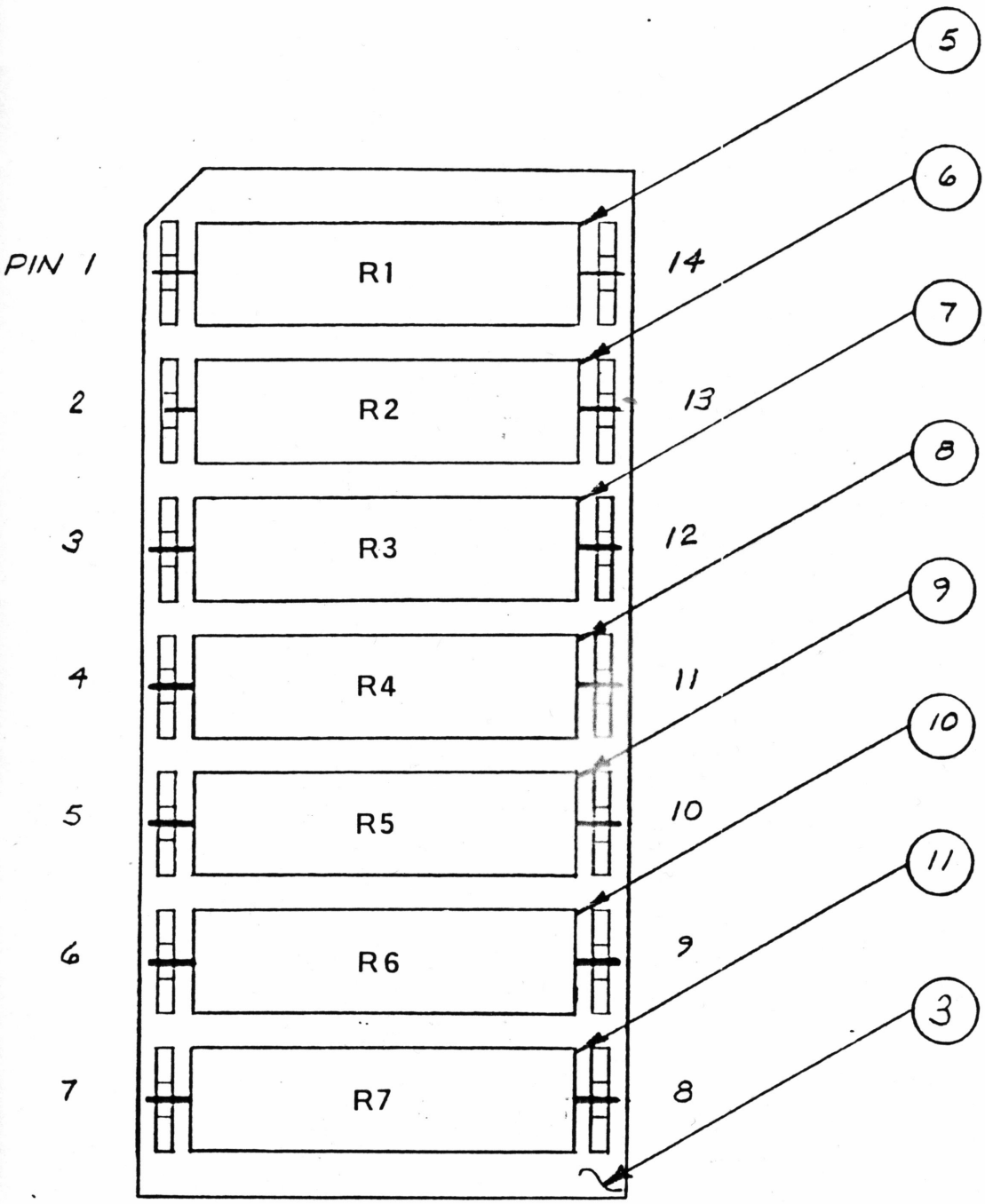


FIGURE 7-15
A1A3A12, COMPONENT MODULE ASSEMBLY
07577301 Rev A

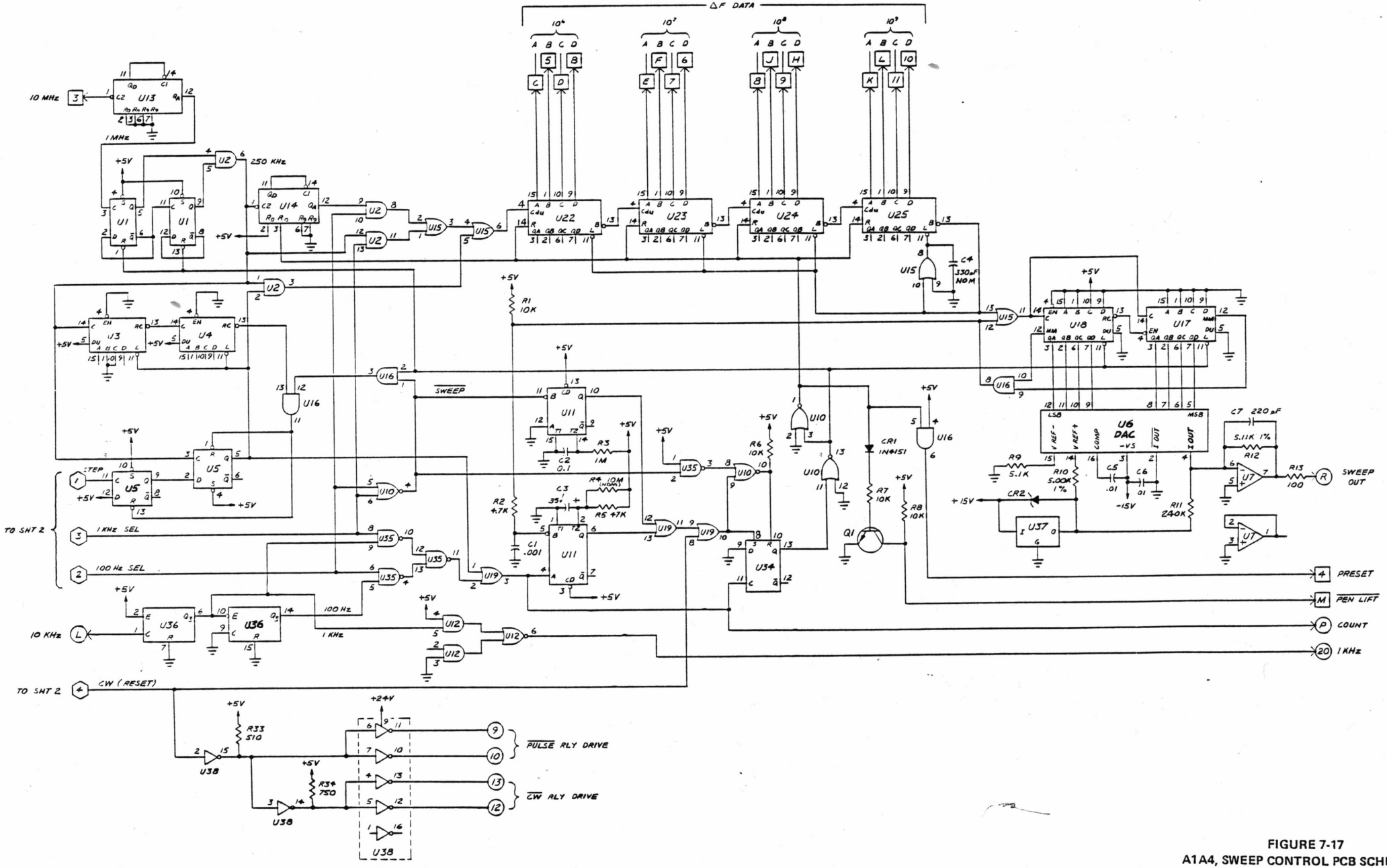


FIGURE 7-17
A1A4, SWEEP CONTROL PCB SCHEMATIC
7-07572701 Rev D (Sheet 1 of 2)

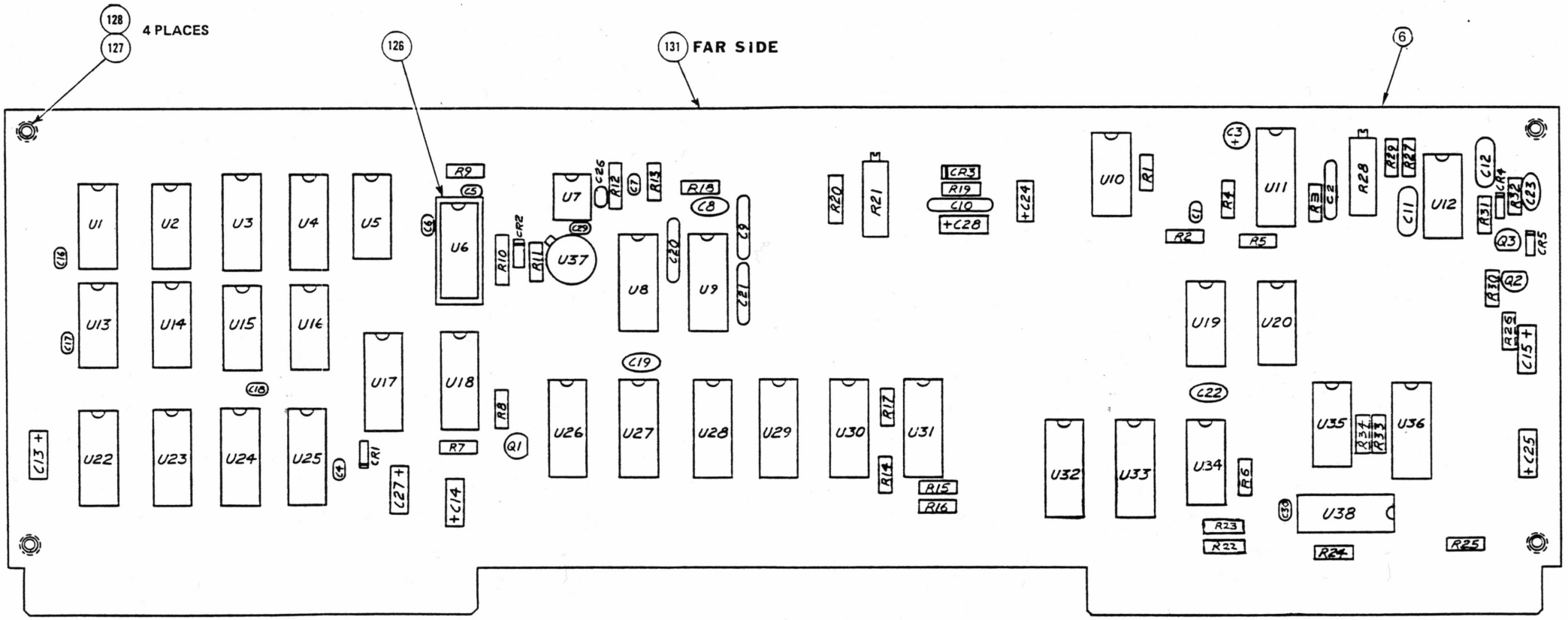
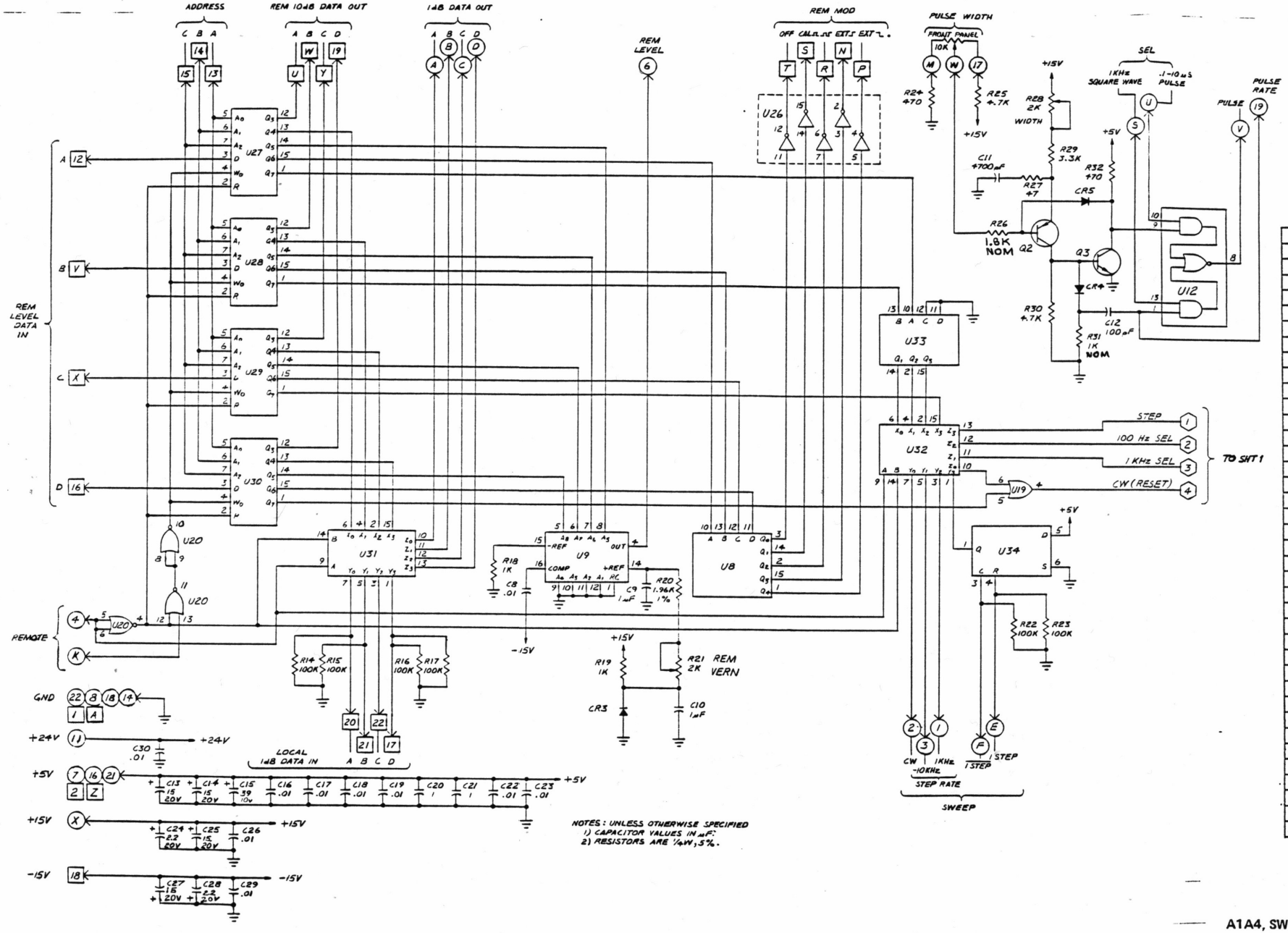


FIGURE 7-16
A1A4, SWEEP CONTROL PCB ASSEMBLY
07572701 Rev G



REF. NO.	TYPE	+5V	-5.2V	+15V	-15V	GND
U39	MC1413P					8
U37	AD581LH					
U36	MC14518BCP	16				8
U35	MCM011BCP	14				7
U34	MC14013BCP	14				7
U33	MC14028BCP	16				8
U32	MC145190CP	16				8
U31	MC145190CP	16				8
U30	CD4099BE	16				8
U29	CD4099BE	16				8
U28	CD4099BE	16				8
U27	CD4099BE	16				8
U26	MC14049BCP	1				8
U25	SN74LS192N	16				8
U24	SN74LS192N	16				8
U23	SN74LS192N	16				8
U22	SN74LS192N	16				8
U21	NOT USED					
U20	MC14001BCP	14				7
U19	MC14071BCP	14				7
U18	SN74LS191N	16				8
U17	SN74LS191N	16				8
U16	SN74LS02N	14				7
U15	SN74LS32N	14				7
U14	SN74LS90N	5				10
U13	SN74LS90N	5				10
U12	SN7451N	14				7
U11	MC14528BCP	16				8
U10	SN74LS02N	14				7
U9	MC1408P7	13			3	2
U8	MC14028BCP	16				8
U7	TL072CP		8	4		
U6	DAC-08	13			3	1
U5	SN74LS74N	14				7
U4	SN74LS191N	16				8
U3	SN74LS191N	16				8
U2	SN74LS08N	14				7
U1	SN74LS74N	14				7

FIGURE 7-17
A1A4, SWEEP CONTROL PCB SCHEMATIC
7-07572701 Rev D (Sheet 2 of 2)

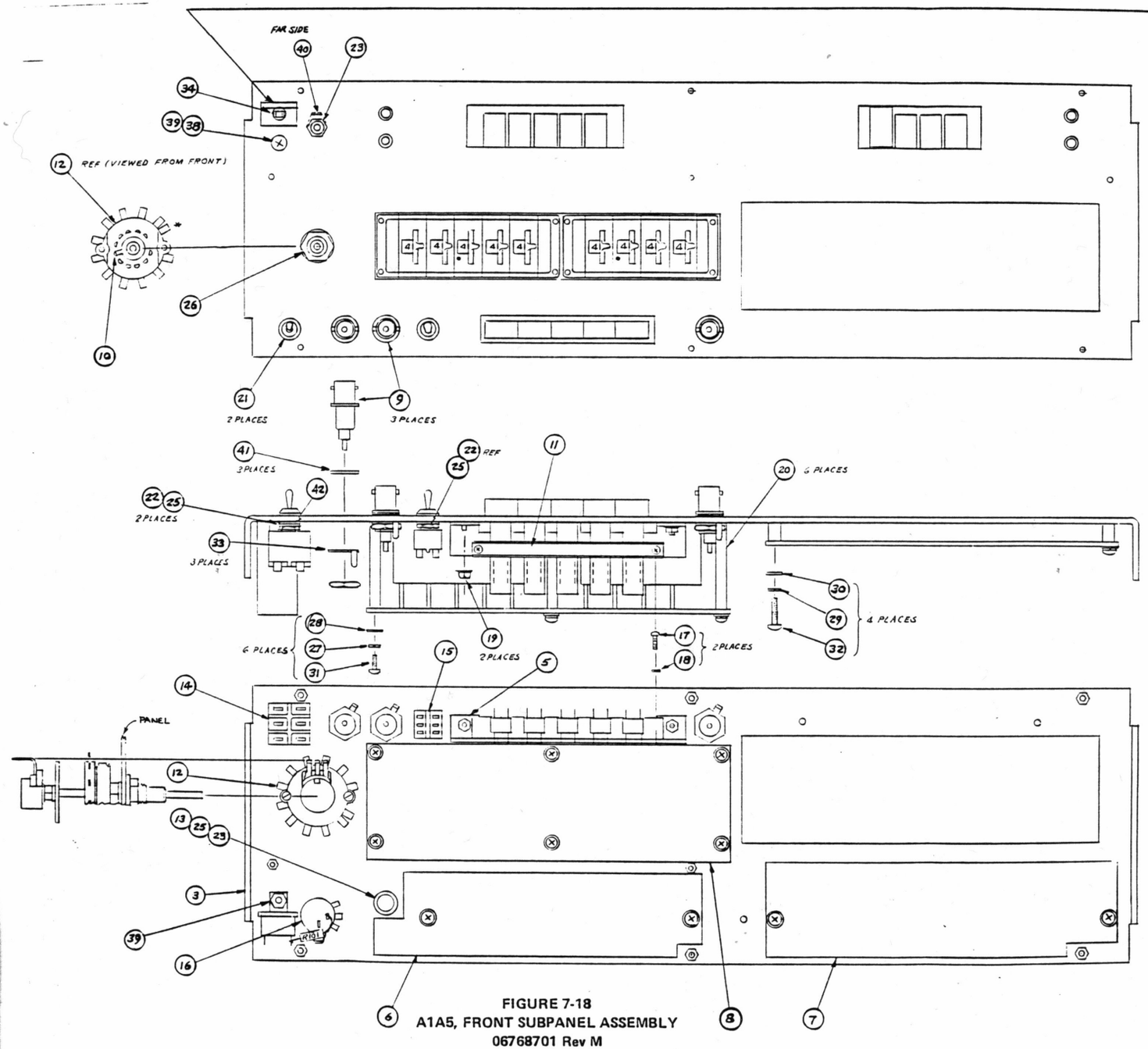


FIGURE 7-18
A1A5, FRONT SUBPANEL ASSEMBLY
06768701 Rev M

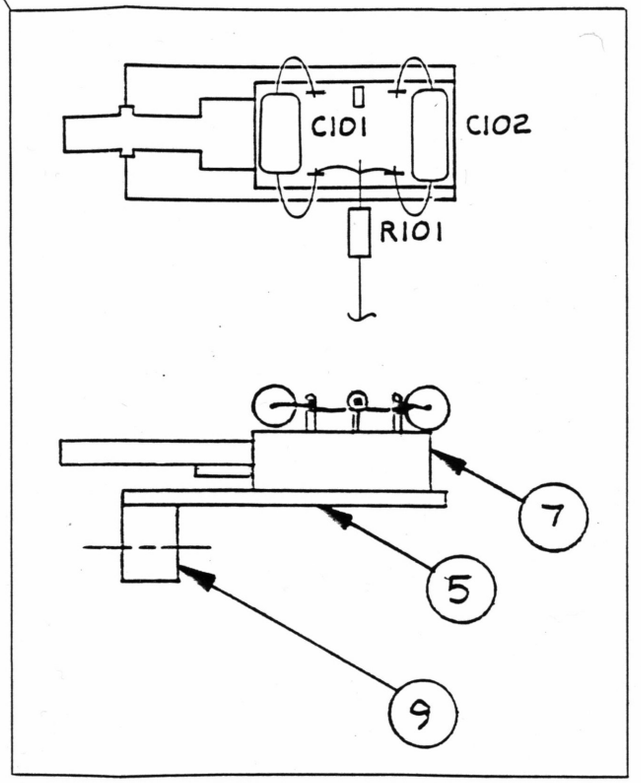


FIGURE 7-19
A1A5A23, PUSHBUTTON SWITCH PCB ASSEMBLY
06783501 Rev B

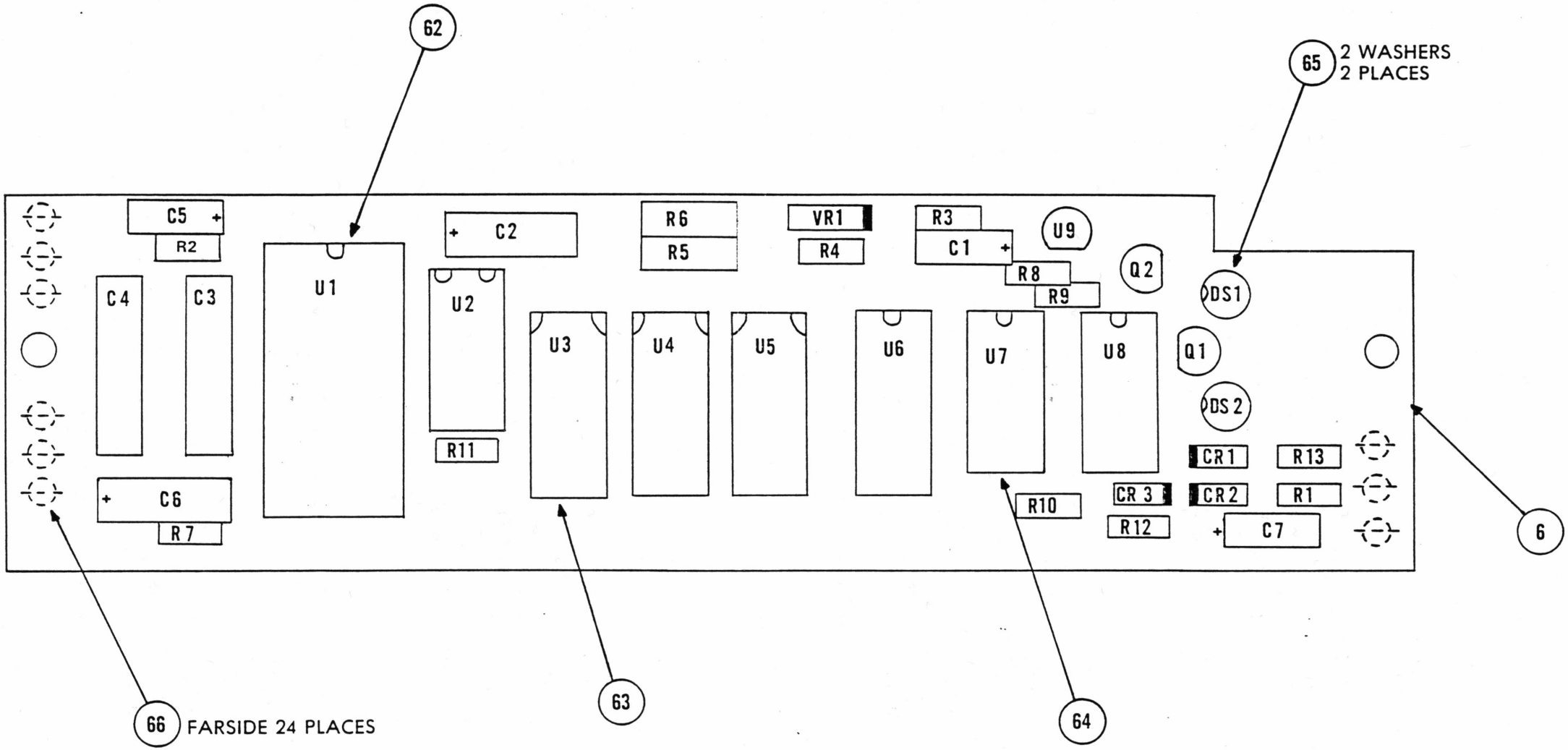
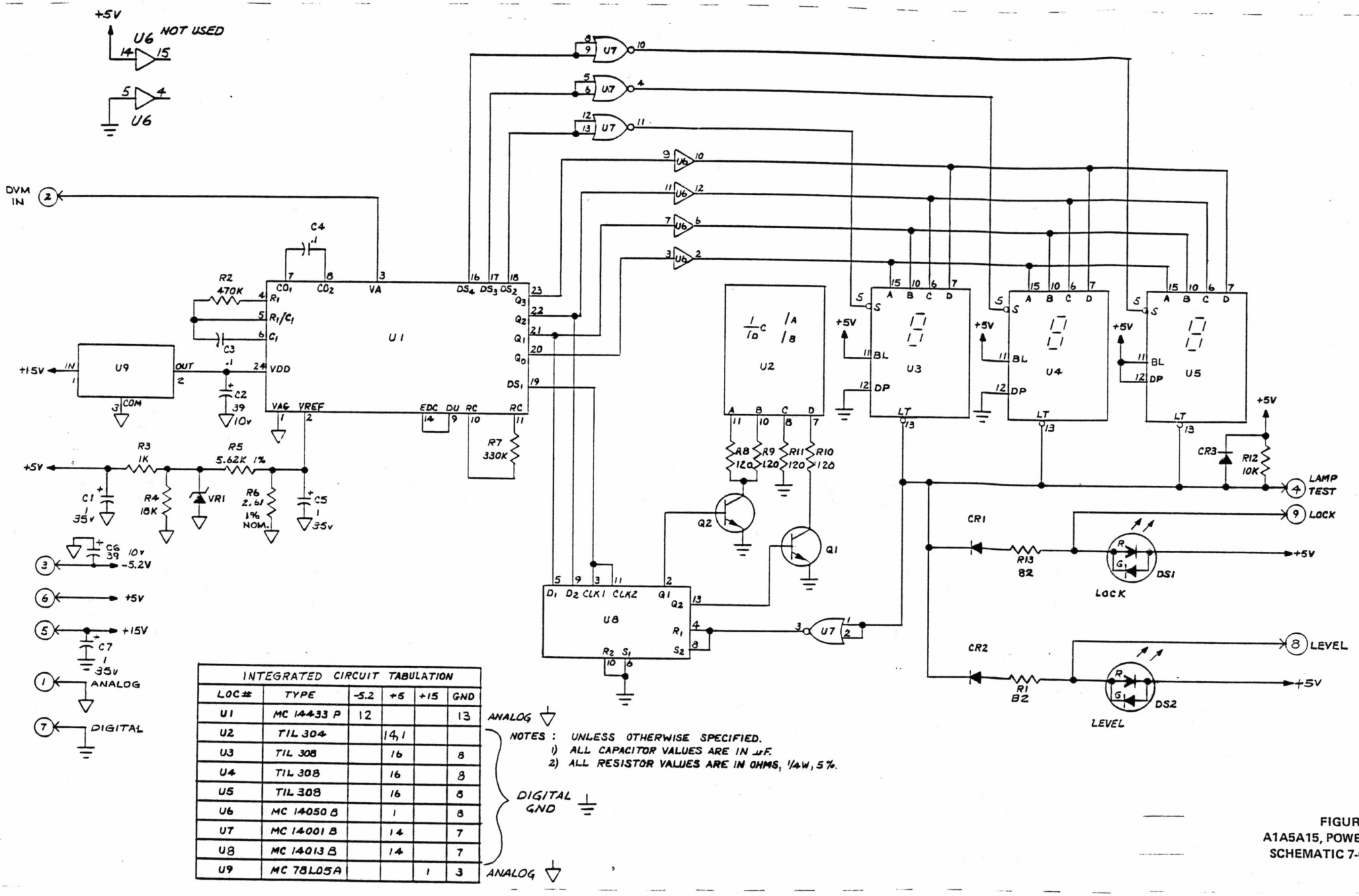


FIGURE 7-20
A1A5A15, POWER DISPLAY PCB
ASSEMBLY 06726801 Rev H



INTEGRATED CIRCUIT TABULATION					
LOC#	TYPE	-5.2	+5	+15	GND
U1	MC 14433 P	12			13
U2	TIL 304		14,1		
U3	TIL 308		16		8
U4	TIL 308		16		8
U5	TIL 308		16		8
U6	MC 14050 B		1		8
U7	MC 14001 B		14		7
U8	MC 14013 B		14		7
U9	MC 78L05A			1	3

NOTES : UNLESS OTHERWISE SPECIFIED.
1) ALL CAPACITOR VALUES ARE IN μF.
2) ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.

FIGURE 7-21
A1A5A15, POWER DISPLAY PCB
SCHEMATIC 7-06726801 Rev G

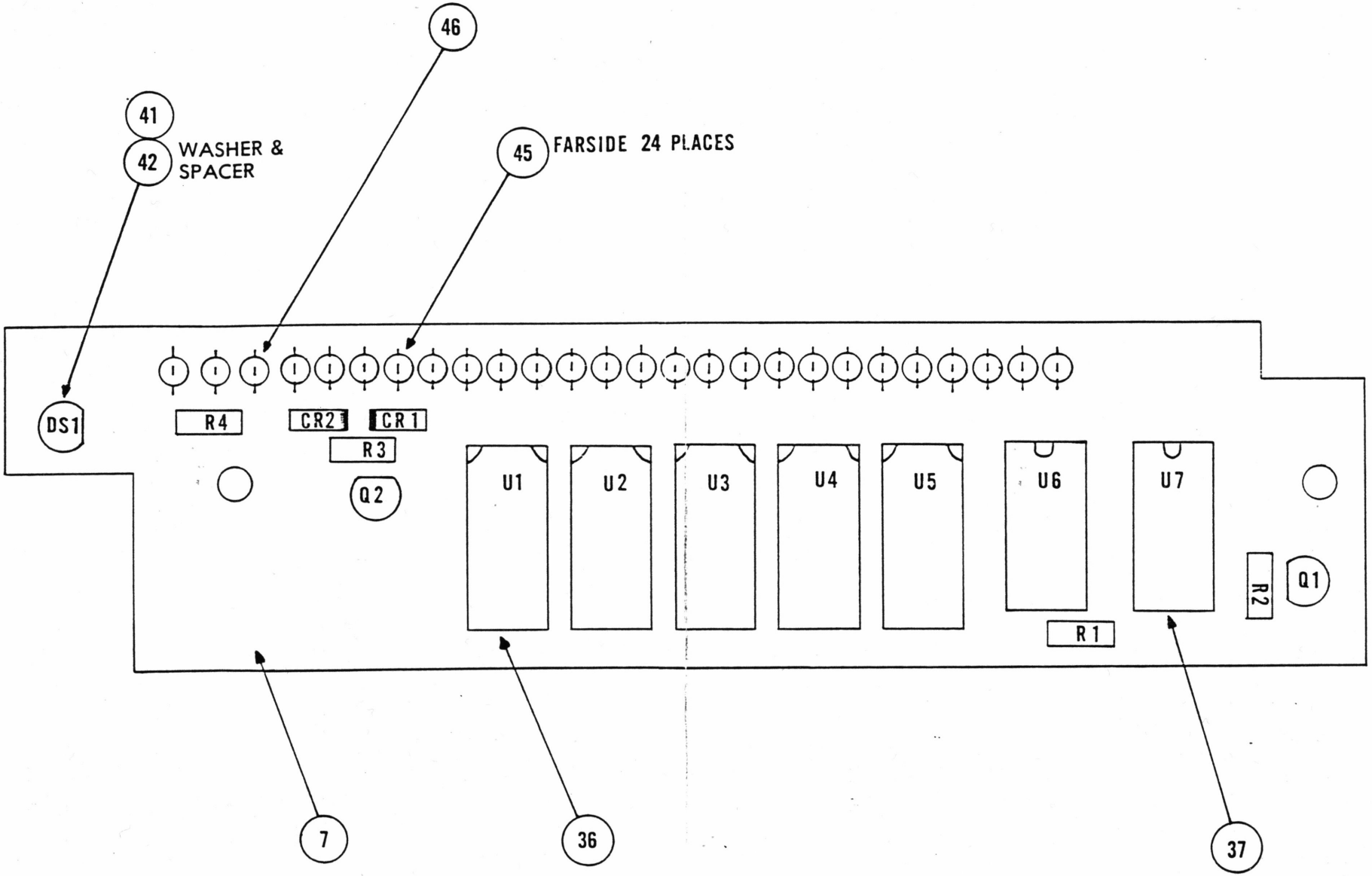
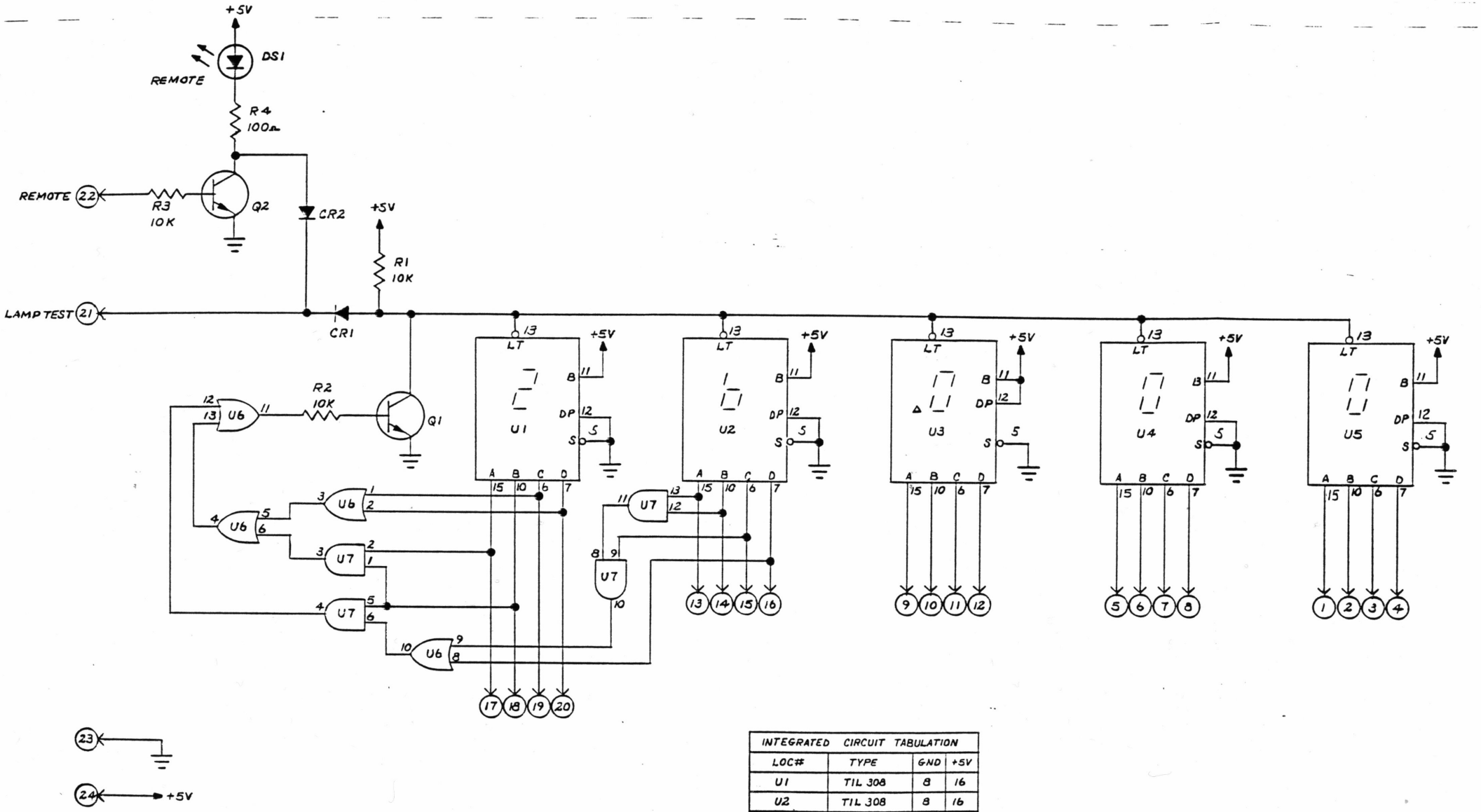


FIGURE 7-22
A1A5A16, FREQUENCY DISPLAY PCB
ASSEMBLY 06726701 Rev F



NOTES: UNLESS OTHERWISE SPECIFIED

1) RESISTORS ARE 1/4W, 5%, CC.

INTEGRATED CIRCUIT TABULATION			
LOC#	TYPE	GND	+5V
U1	TIL 308	8	16
U2	TIL 308	8	16
U3	TIL 308	8	16
U4	TIL 308	8	16
U5	TIL 308	8	16
U6	MC 14071BCP	7	14
U7	MC 14081BCP	7	14

FIGURE 7-23
A1A5A16, FREQUENCY DISPLAY PCB
SCHEMATIC 7-06726701 Rev C

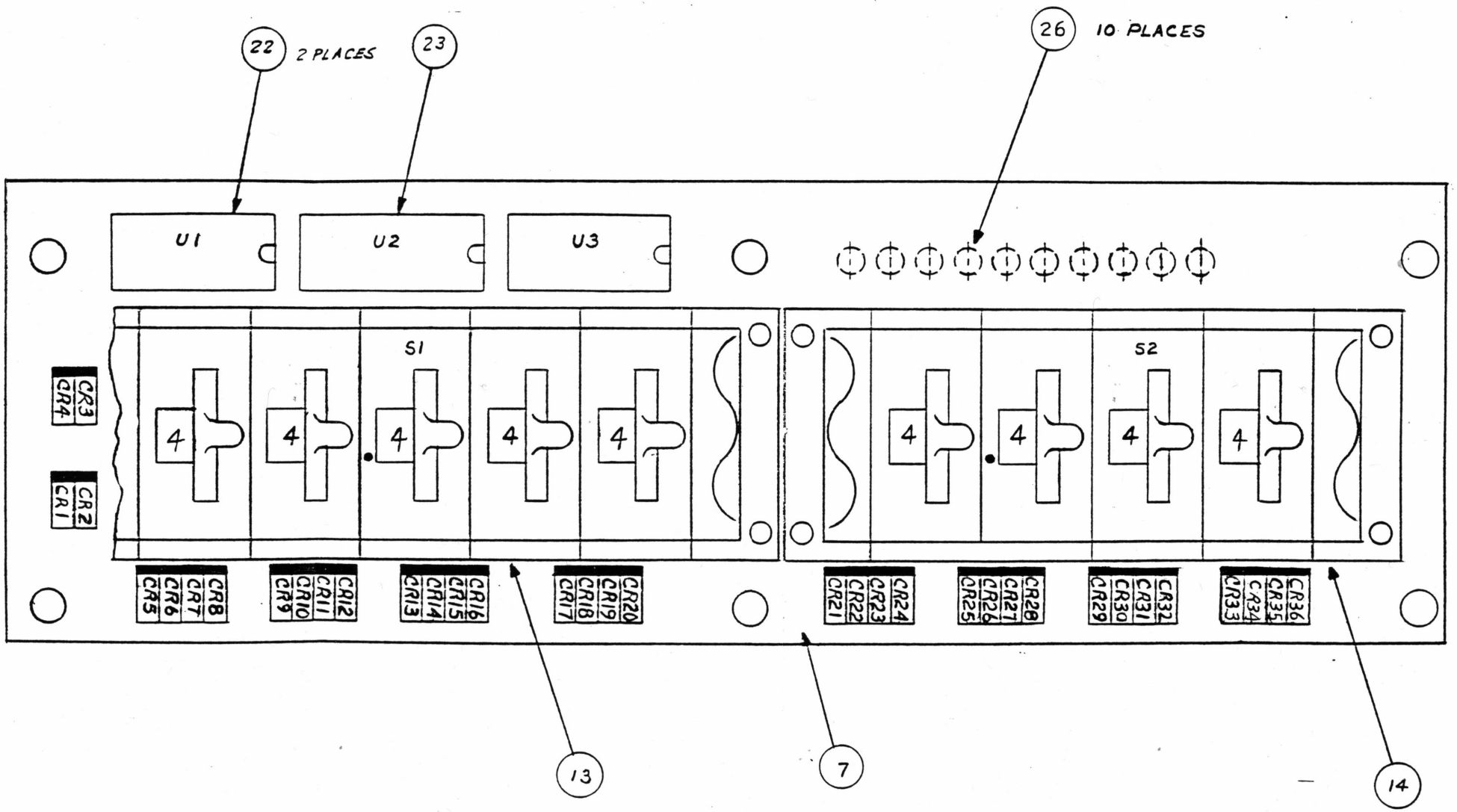


FIGURE 7-24
A1A5A17, LEVER SWITCH PCB
ASSEMBLY 06729401 Rev B

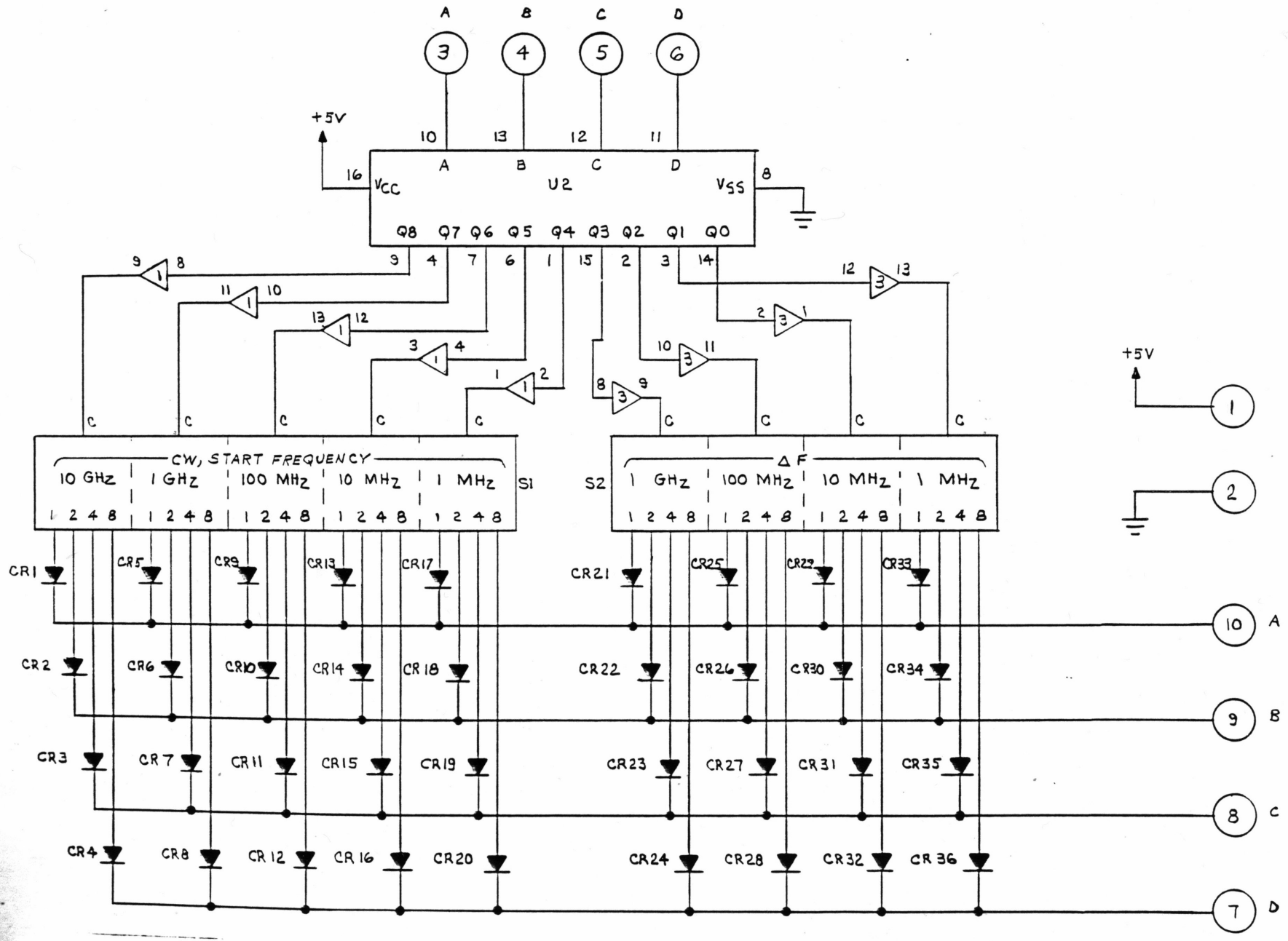
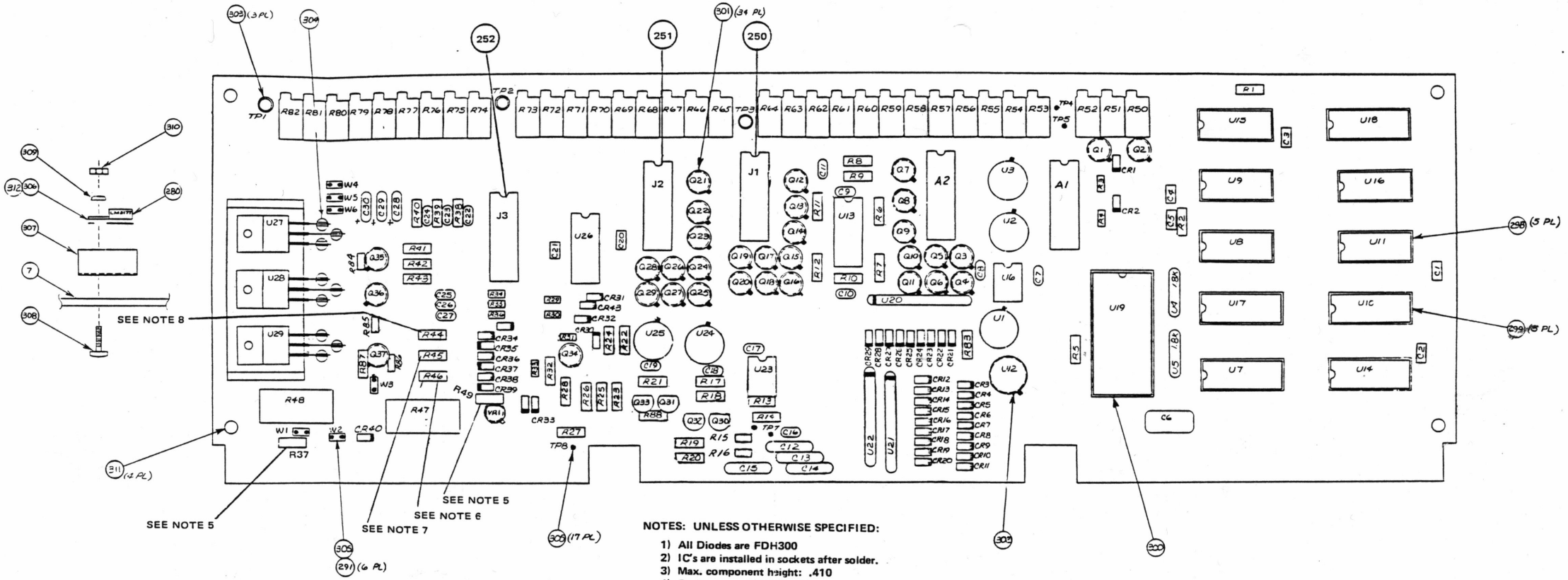


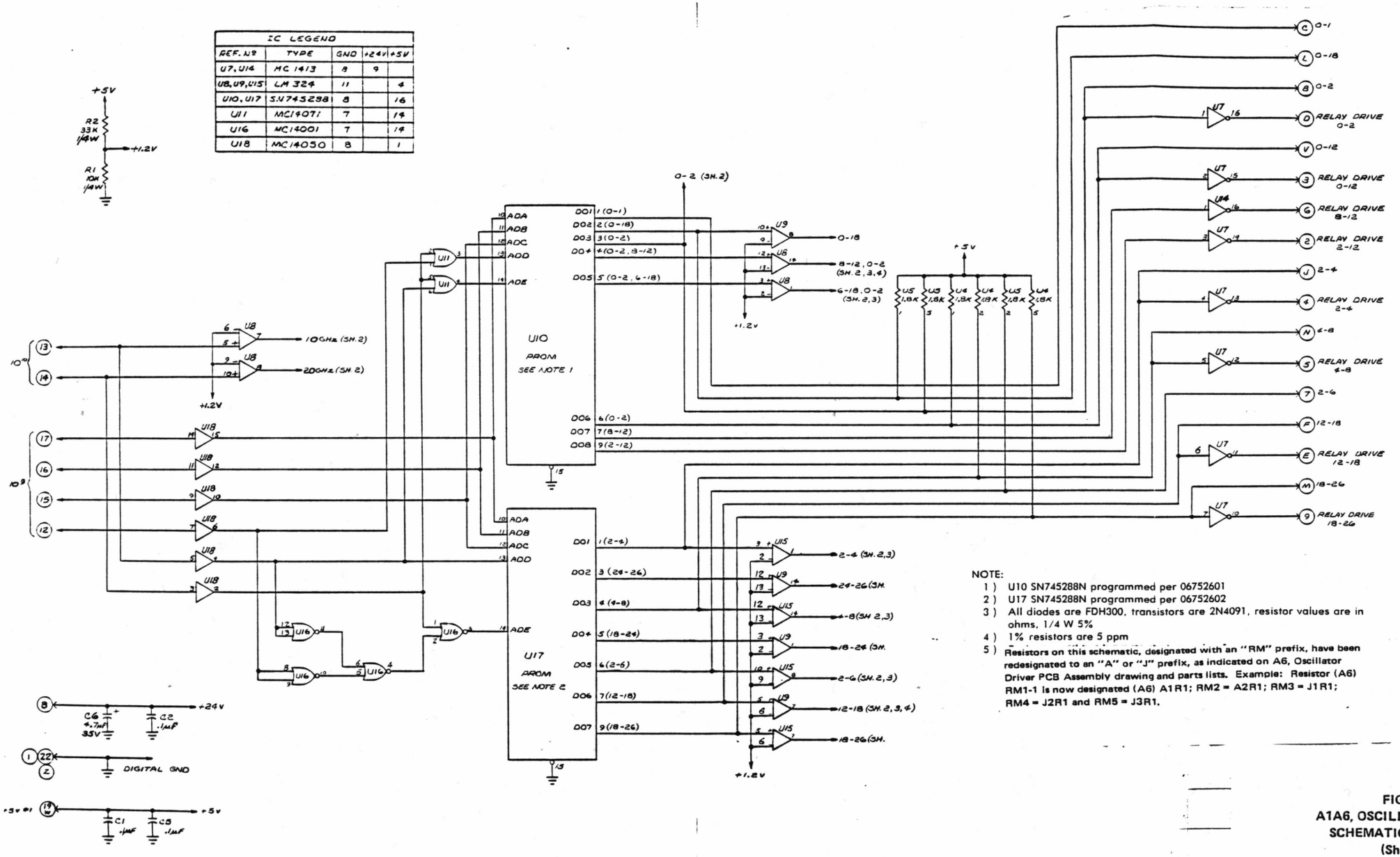
FIGURE 7-25
A1A5A17, LEVER SWITCH PCB
SCHEMATIC 7-06729401 Rev A



NOTES: UNLESS OTHERWISE SPECIFIED:

1) All Diodes are FDH300
2) IC's are installed in sockets after solder.
3) Max. component height: .410
4) Resistors are 1/4W 5%, CC
5) Resistors R37 and R49 are part of the 4 to 8.7 GHz Oscillator Kit (Part No. 077191) and are shown here only to identify their installed location.
6) Resistor R46 is part of the 12 to 18 GHz Oscillator Kit (Part No. 077194) and the alternate 12 to 18 GHz Oscillator Kit (Part No. 077195) and is shown here only to identify its installed location.
7) Resistor R45 is part of the 8 to 12 GHz Oscillator Kit (Part No. 077196) and the non-alternate 8 to 12 GHz Oscillator Kit (Part No. 077198) and is shown here only to identify its installed location.
8) Resistor R44 is part of the 18 to 26 GHz Oscillator Kit (Part No. 077197) and is shown here only to identify its installed location.

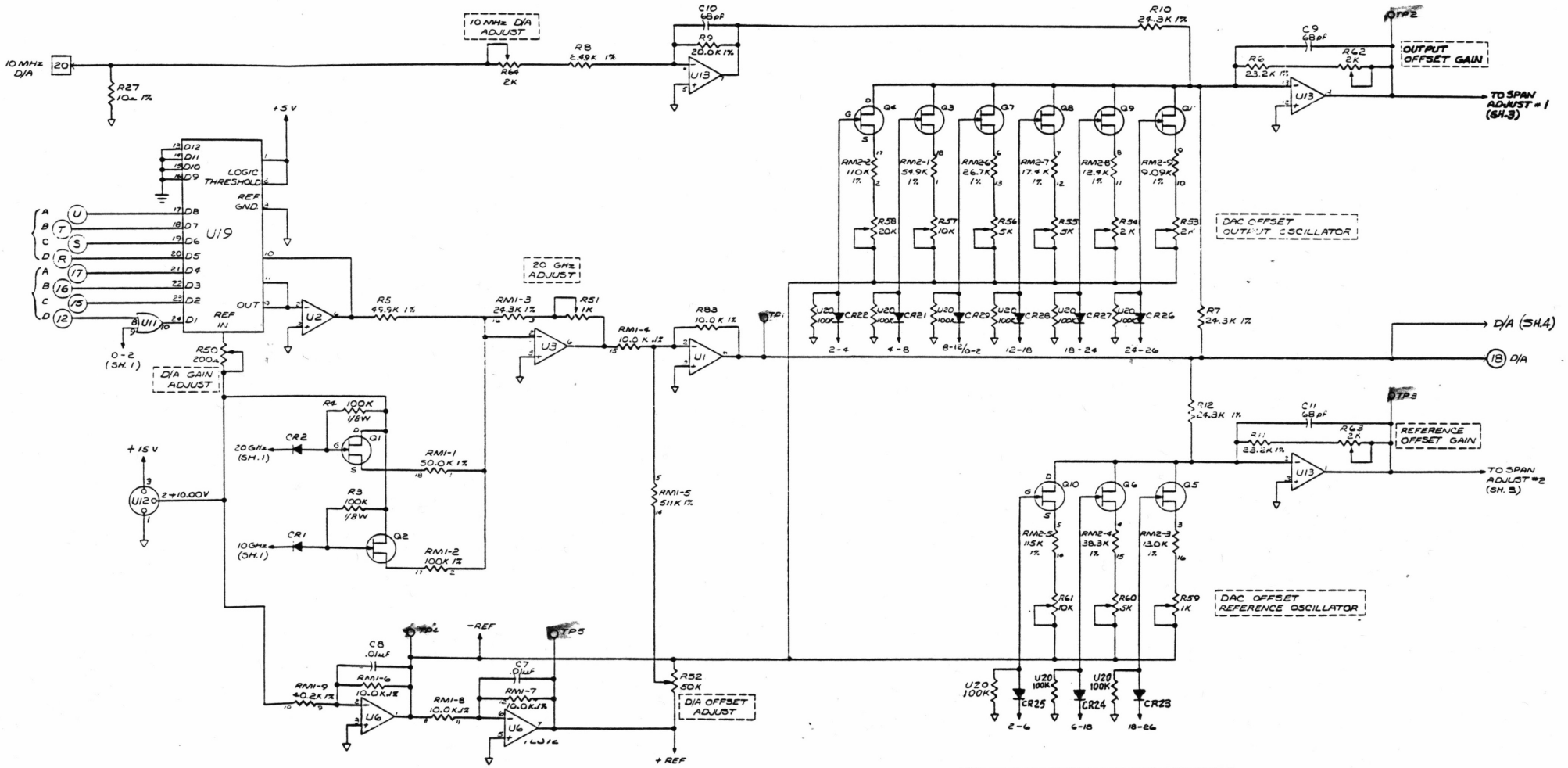
FIGURE 7-26
A1A6, OSCILLATOR DRIVER PCB
ASSEMBLY 07559601 Rev F



NOTE:

1) U10 SN745288N programmed per 06752601
2) U17 SN745288N programmed per 06752602
3) All diodes are FDH300, transistors are 2N4091, resistor values are in ohms, 1/4 W 5%
4) 1% resistors are 5 ppm
5) Resistors on this schematic, designated with an "RM" prefix, have been redesignated to an "A" or "J" prefix, as indicated on A6, Oscillator Driver PCB Assembly drawing and parts lists. Example: Resistor (A6) RM1-1 is now designated (A6) A1R1; RM2 = A2R1; RM3 = J1R1; RM4 = J2R1 and RM5 = J3R1.

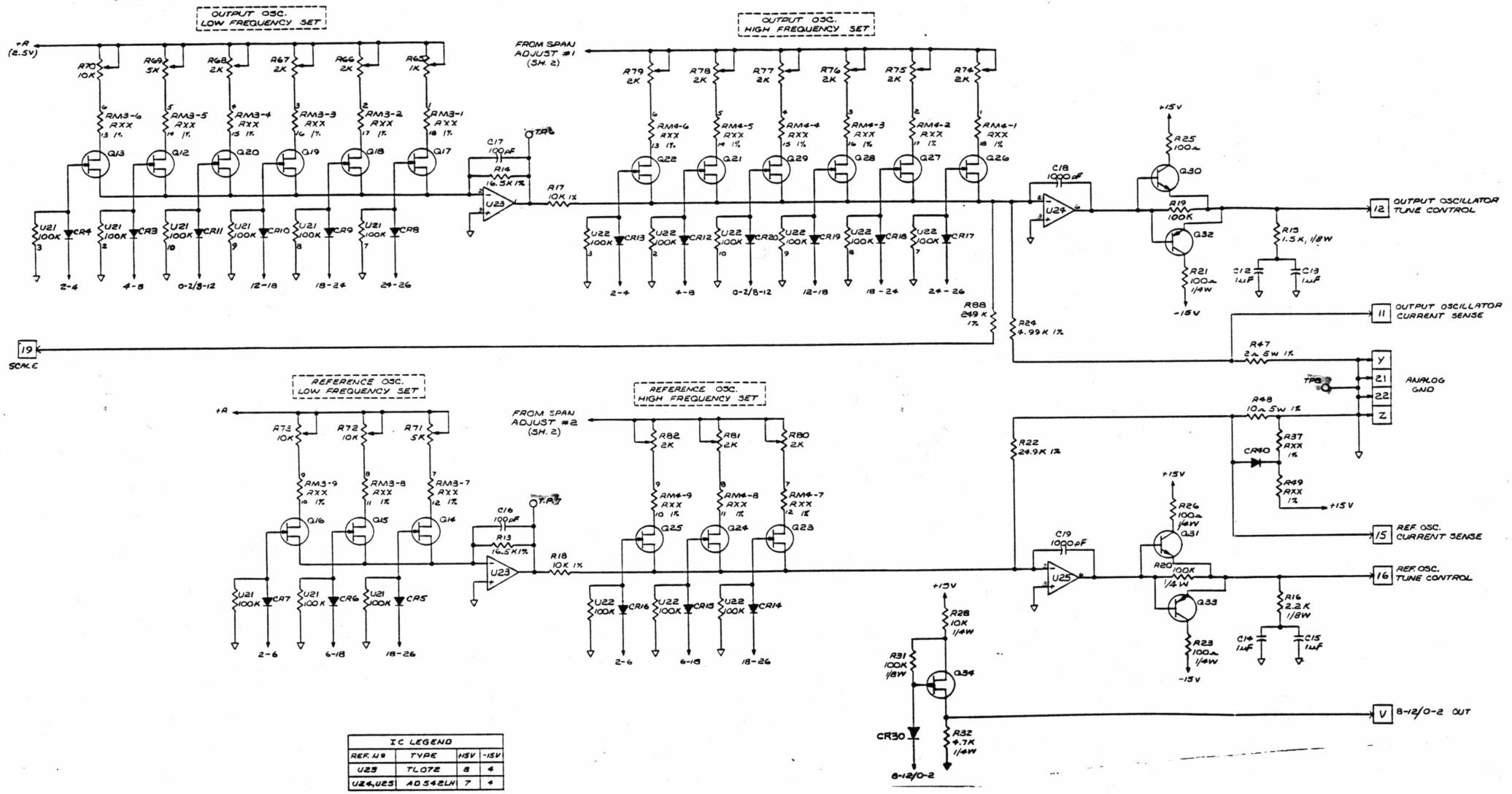
FIGURE 7-27
A1A6, OSCILLATOR DRIVER PCB
SCHEMATIC 7-07559601 Rev C
(Sheet 1 of 4)



IC LEGEND						
REF. Nº	TYPE	GND	+5V	+15V	-15V	+10.00 V OUT
U1, U2, U3	AD 542 LH			7	4	
U6	TL072			8	4	
U12	AD581LH	1		3		2
U13	TL074			4	11	
U19	AD5G2KD	12	1		6	

NOTE:
Resistors on this schematic, designated with an "RM" prefix, have been redesignated to an "A" prefix, as indicated on A6, Oscillator Driver PCB Assembly drawing and parts lists. Example: Resistor (A6) RM1-1 is now designated (A6) A1R1.

FIGURE 7-27
A1A6, OSCILLATOR DRIVER PCB
SCHEMATIC 7-07559601 Rev C
(Sheet 2 of 4)



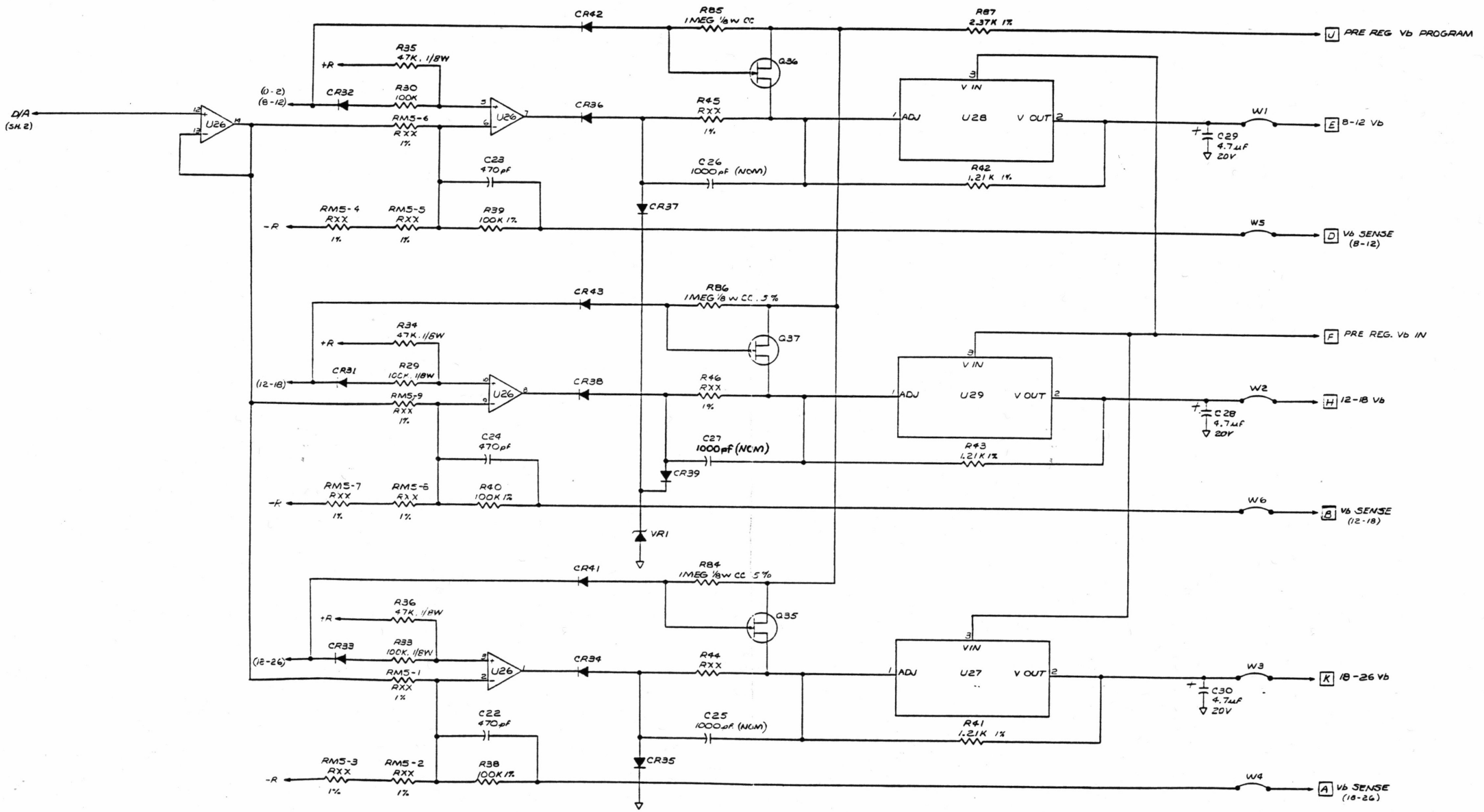
IC LEGEND			
REF. NO	TYPE	+15V	-15V
U23	TL072	8	4
U24,U25	AD542LH	7	4

NOTE: RXX VALUES SELECTED TO MATCH INDIVIDUAL OSCILLATOR REQUIREMENTS.

NOTE:
Resistors on this schematic, designated with an "RM" prefix, have been redesignated to an "A" prefix, as indicated on A6, Oscillator Driver PCB Assembly drawing and parts lists. Example: Resistor (A6) RM1-1 is now designated (A6) A1R1.

FIGURE 7-27
A1A6, OSCILLATOR DRIVER PCB
SCHEMATIC 7-07559601 Rev C
(Sheet 3 of 4)

Q_1-Q_{29} 2N4091 J-FET
Q_{30}-Q_{34} 2N3904 NPN



NOTE:
Resistors on this schematic, designated with an "RM" prefix, have been redesignated to an "A" prefix, as indicated on A6, Oscillator Driver PCB Assembly drawing and parts lists. Example: Resistor (A6) RM1-1 is now designated (A6) A1R1.

IC LEGEND						
REF. NO	TYPE	+6V	+15V	ADJ	V_{OUT}	V_{IN}
U26	LM324	11	4			
U27,U28,U29	LM317T			1	2	3

FIGURE 7-27
A1A6, OSCILLATOR DRIVER PCB
SCHEMATIC 7-07559601 Rev C
(Sheet 4 of 4)

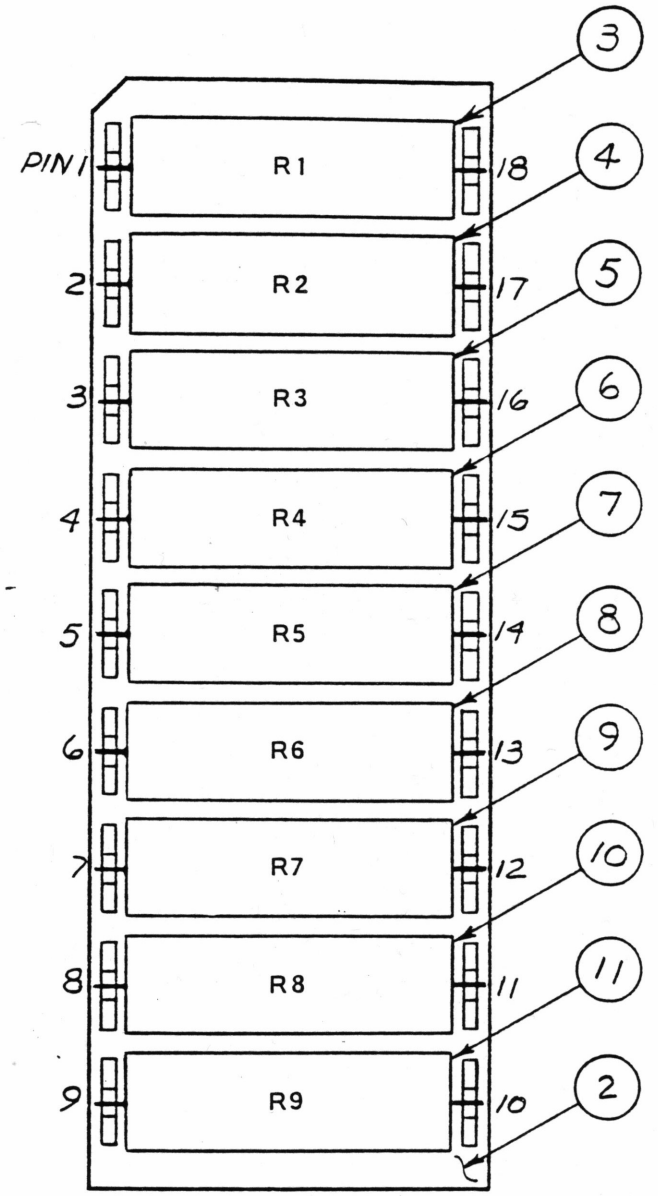


FIGURE 7-28
A1A6A1, A1A6A2, A1A6J1, A1A6J2 and A1A6J3
COMPONENT MODULE ASSEMBLIES
07564201 Rev A, 07564401 Rev A and 07564501 Rev A

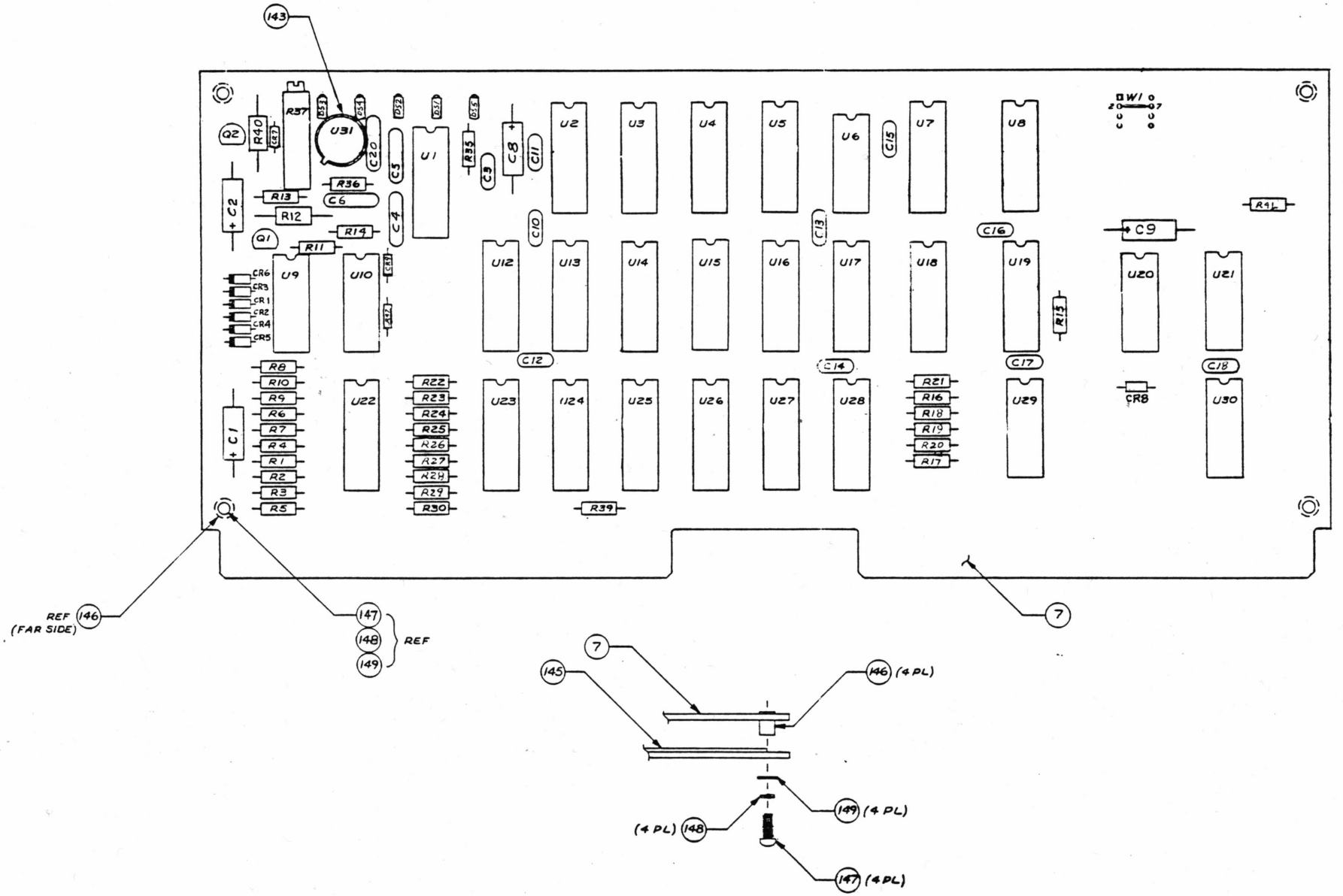
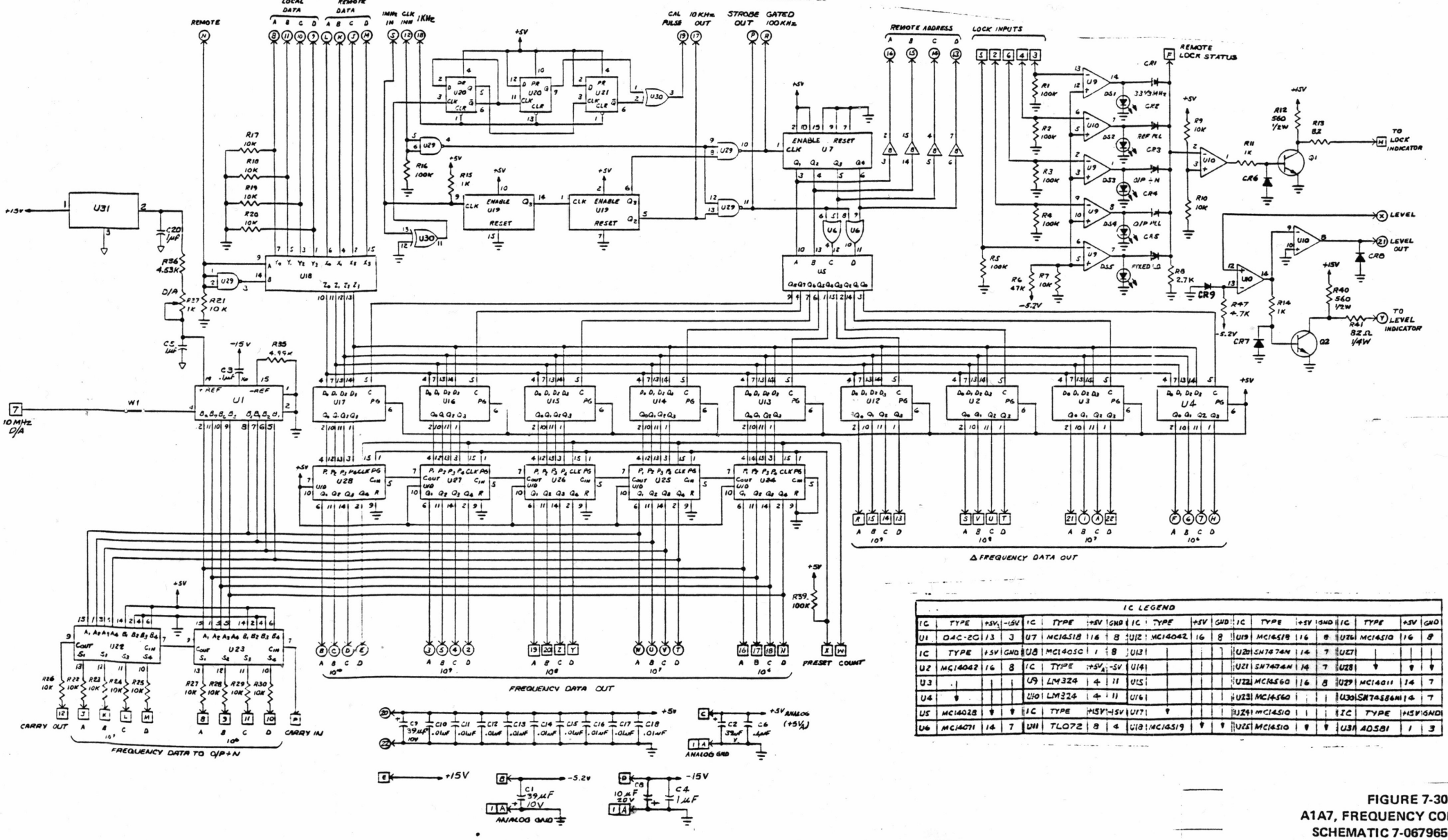


FIGURE 7-29
A1A7, FREQUENCY CONTROL PCB
ASSEMBLY 06796501 Rev N



IC LEGEND																		
IC	TYPE	+5V	-15V	IC	TYPE	+5V	GND	IC	TYPE	+5V	GND	IC	TYPE	+5V	GND	IC	TYPE	+5V	GND
U1	DAC-2C	13	3	U7	MC14518	16	8	U12	MC14042	16	8	U19	MC14518	16	8	U26	MC14510	16	8
IC	TYPE	+5V	GND	U8	MC14056	1	8	U13				U20	SN7474N	14	7	U27			
U2	MC14042	16	8	IC	TYPE	+5V	-5V	U14				U21	SN7474N	14	7	U28			
U3				U9	LM324	4	11	U15				U22	MC14560	16	8	U29	MC14011	14	7
U4				U10	LM324	4	11	U16				U23	MC14560			U30	SN74S86N	14	7
U5	MC14028			IC	TYPE	+15V	-15V	U17				U24	MC14510			IC	TYPE	+15V	GND
U6	MC14071	14	7	U11	TL072	8	4	U18	MC14519			U25	MC14510			U31	AD581	1	3

FIGURE 7-30
A1A7, FREQUENCY CONTROL PCB
SCHEMATIC 7-06796501 Rev M

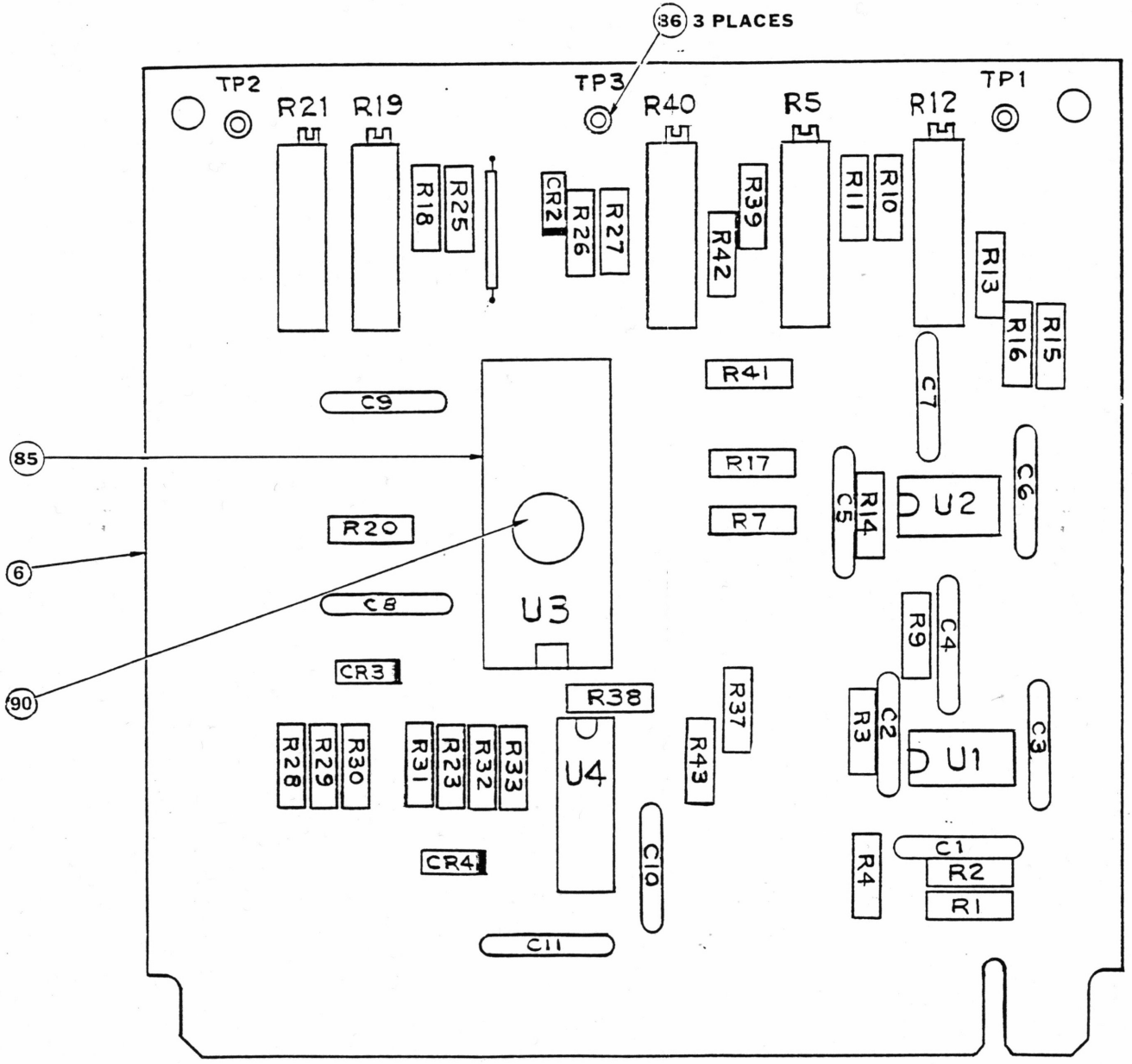
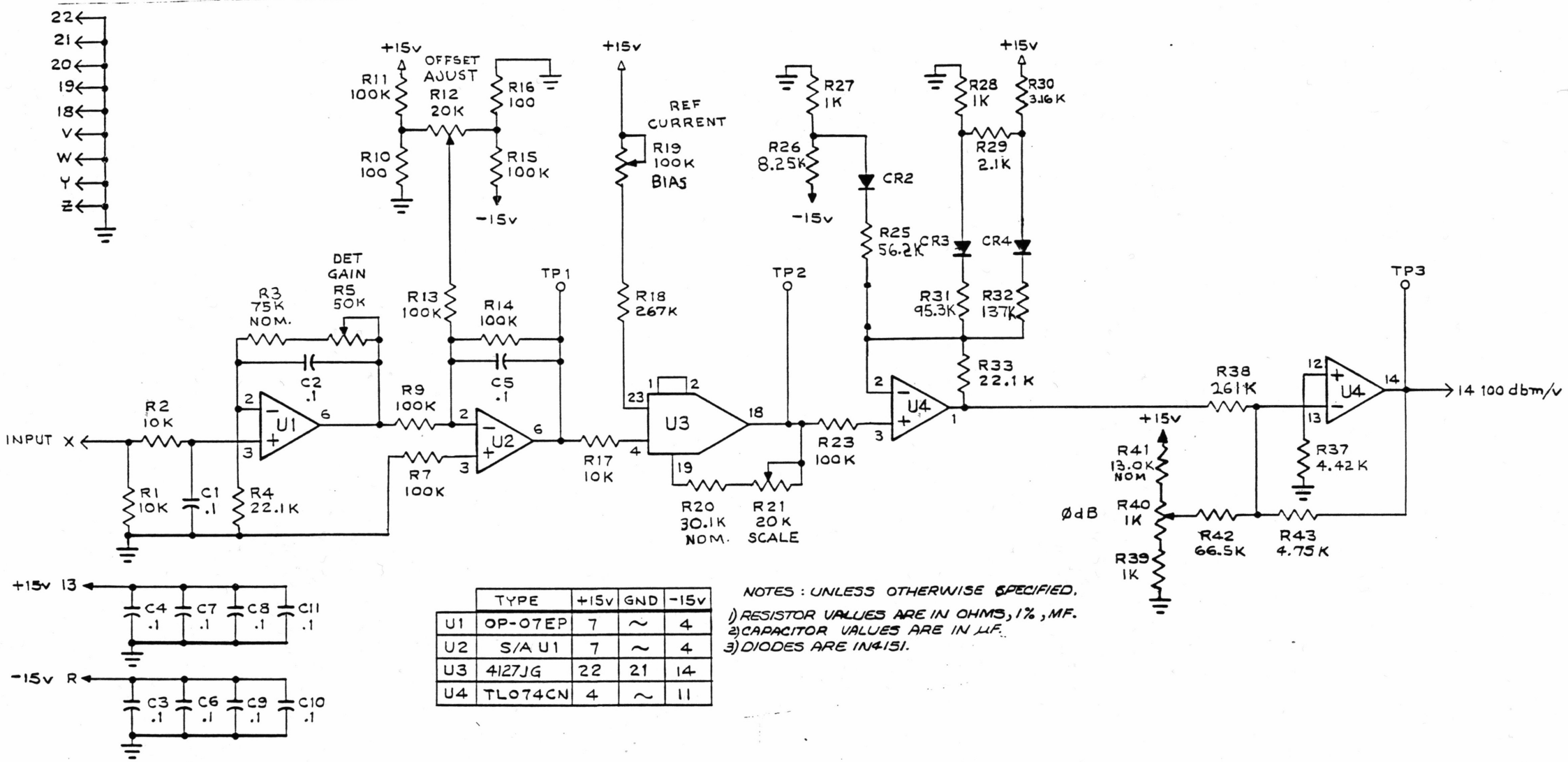


FIGURE 7-31
A1A8, POWER METER PCB
ASSEMBLY 07575201 Rev C



	TYPE	+15v	GND	-15v
U1	OP-07EP	7	~	4
U2	S/A U1	7	~	4
U3	4127JG	22	21	14
U4	TL074CN	4	~	11

NOTES : UNLESS OTHERWISE SPECIFIED.

1) RESISTOR VALUES ARE IN OHMS, 1%, MF.
2) CAPACITOR VALUES ARE IN μF.
3) DIODES ARE IN4151.

FIGURE 7-32
A1A8, POWER METER PCB
SCHEMATIC 7-07575201 Rev C

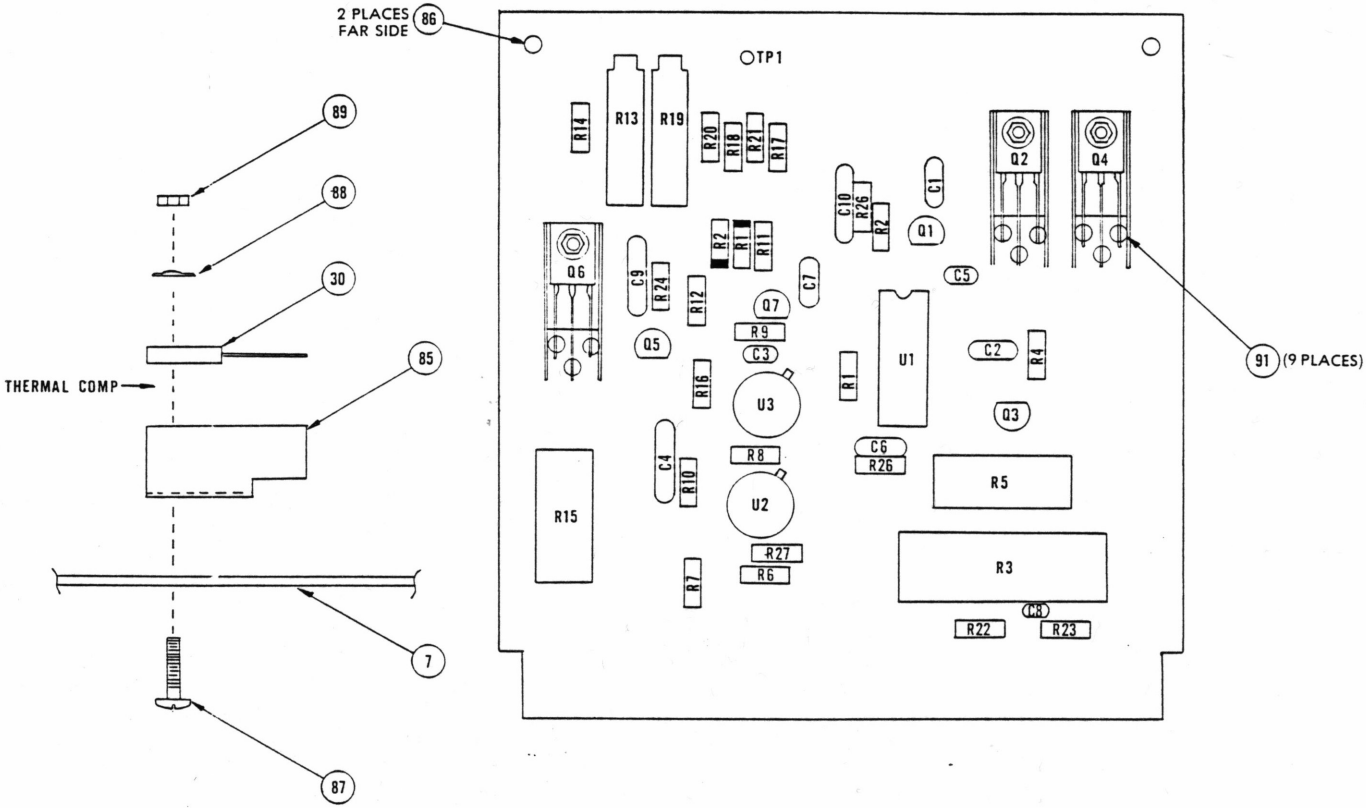


FIGURE 7-33
A1A9, YIG FILTER/FM DRIVER PCB
ASSEMBLY 07558901 Rev E

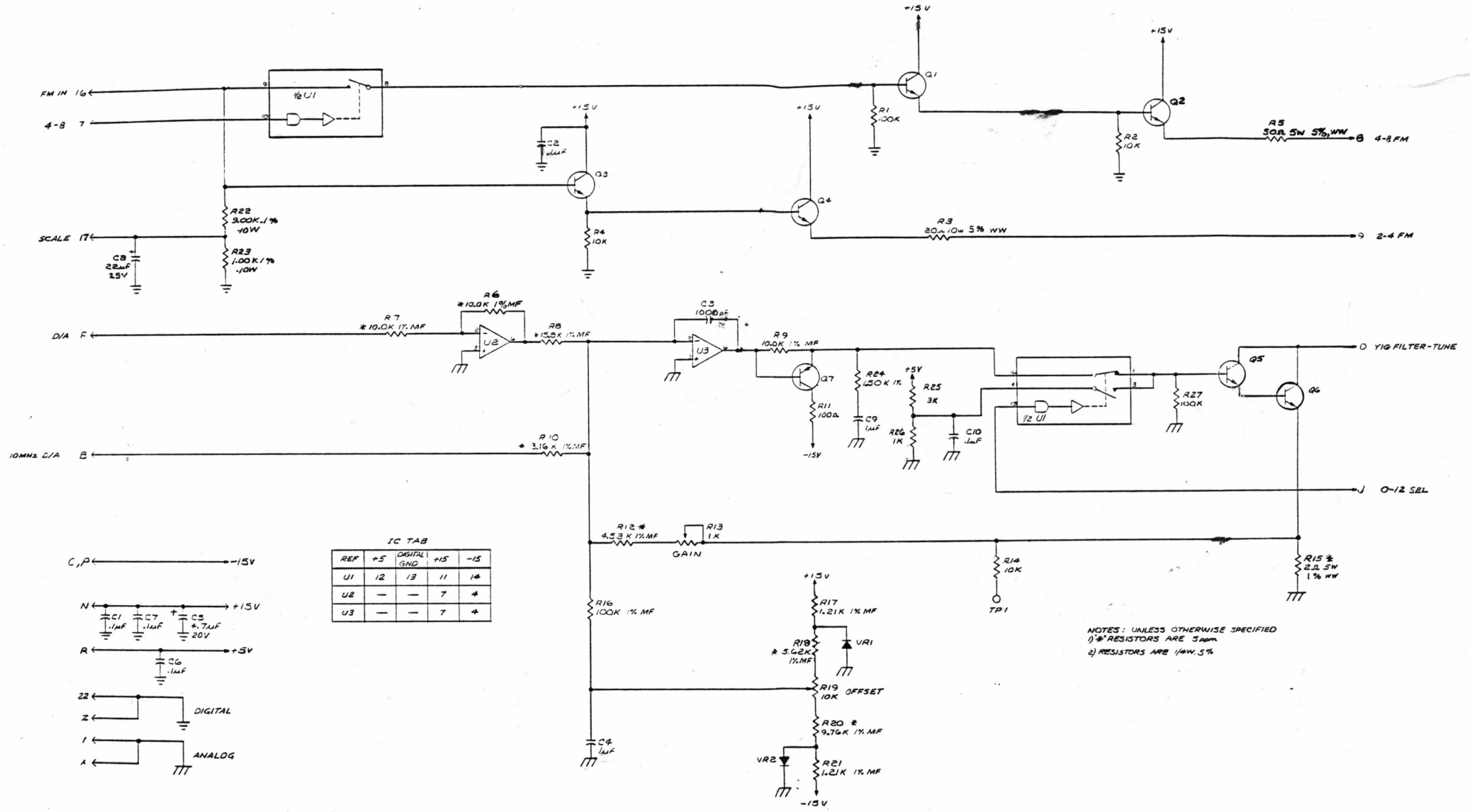


FIGURE 7-34
A1A9, YIG FILTER/FM DRIVER PCB
SCHEMATIC 7-07558901 Rev E

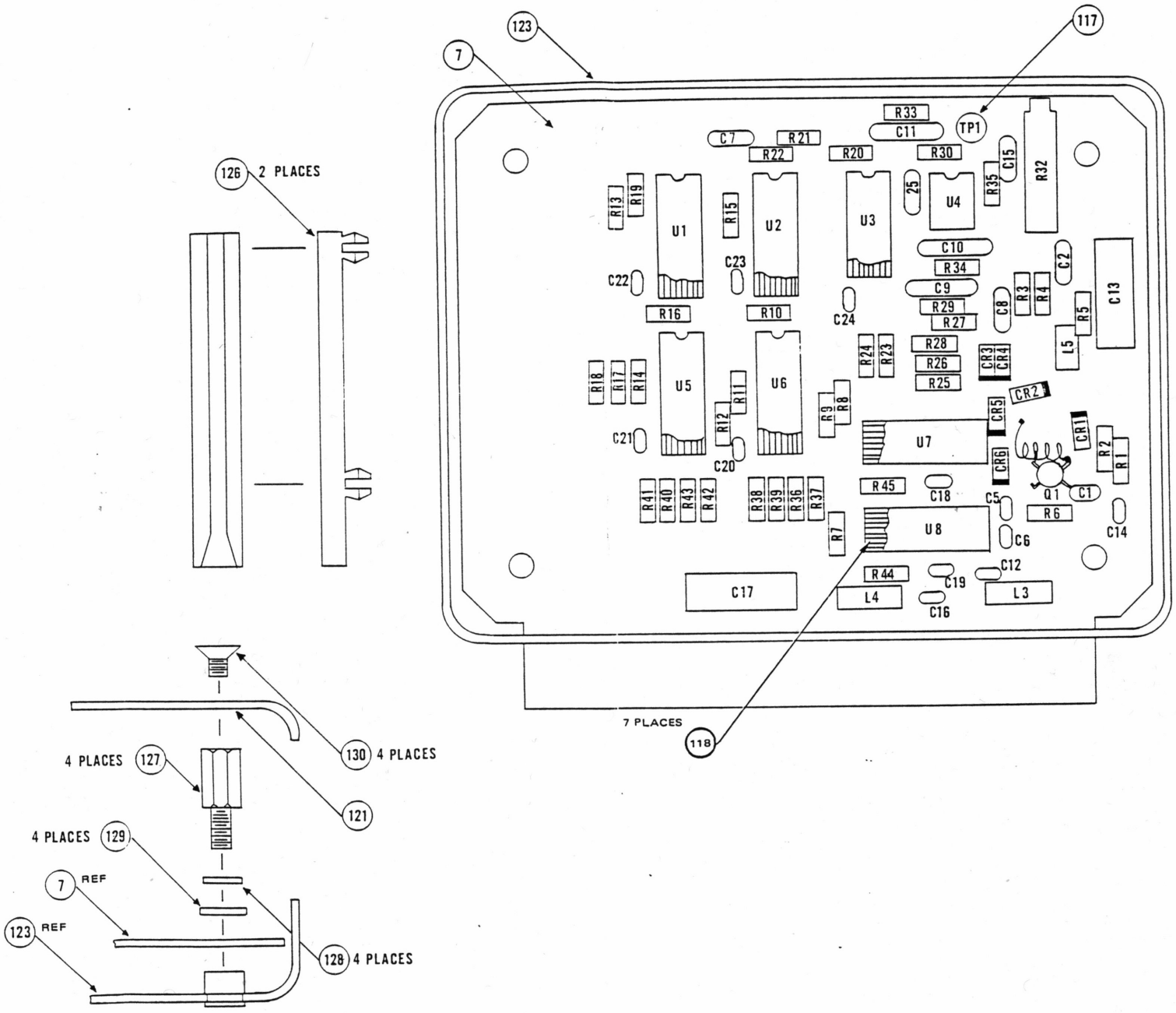
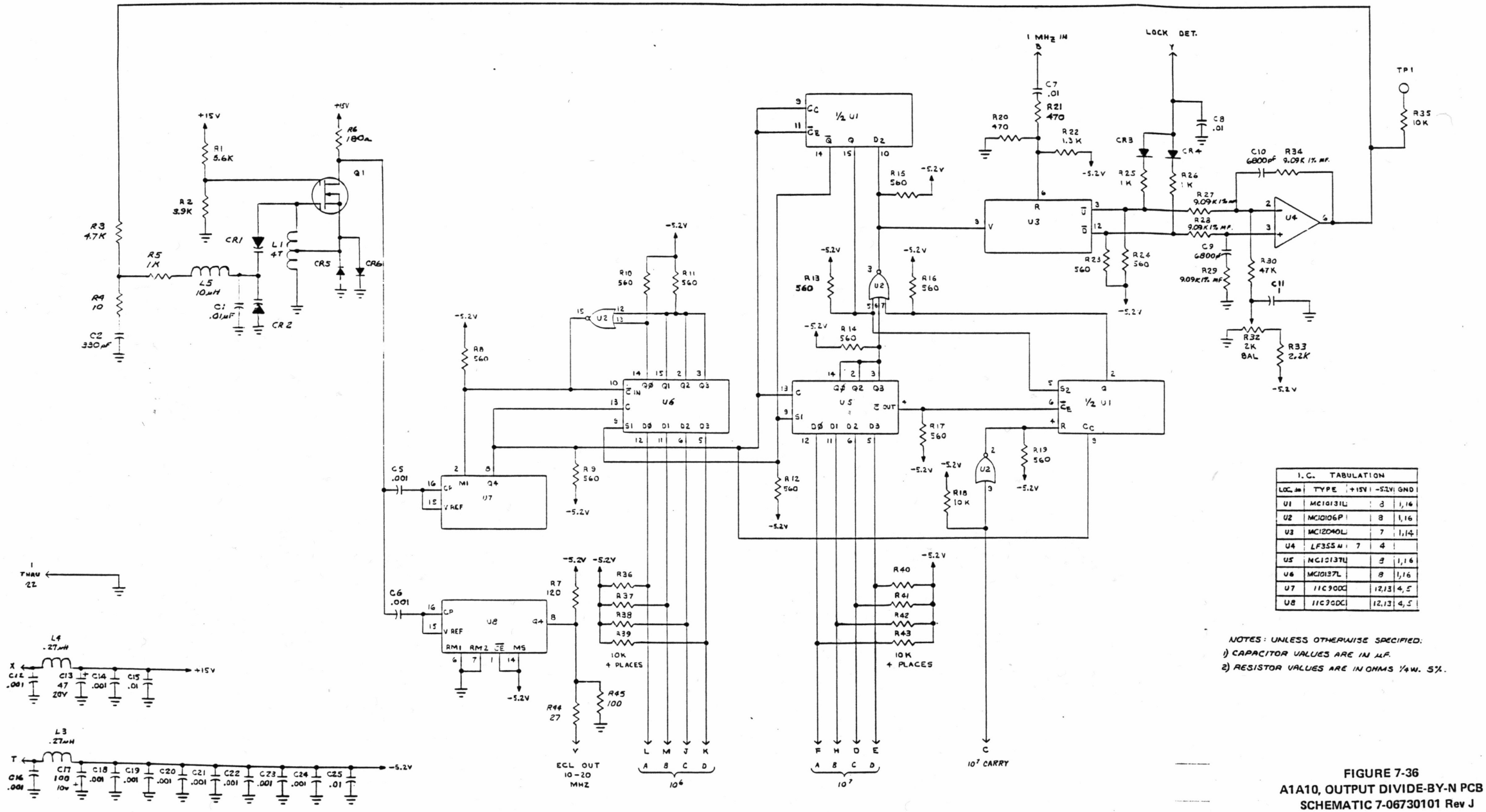


FIGURE 7-35
A1A10, OUTPUT DIVIDE-BY-N PCB
ASSEMBLY 06730101 Rev H



I. C. TABULATION				
LOC. No.	TYPE	+15V	-5.2V	GND
U1	MC10131L	8		1,16
U2	MC10106P	8		1,16
U3	MC12040L	7		1,14
U4	LF355N	7	4	
U5	MC10137L	8		1,16
U6	MC10137L	8		1,16
U7	11C900C	12,13		4,5
U8	11C90DC	12,13		4,5

NOTES: UNLESS OTHERWISE SPECIFIED:
1) CAPACITOR VALUES ARE IN μF.
2) RESISTOR VALUES ARE IN OHMS ¼W. 5%.

FIGURE 7-36
A1A10, OUTPUT DIVIDE-BY-N PCB
SCHEMATIC 7-06730101 Rev J

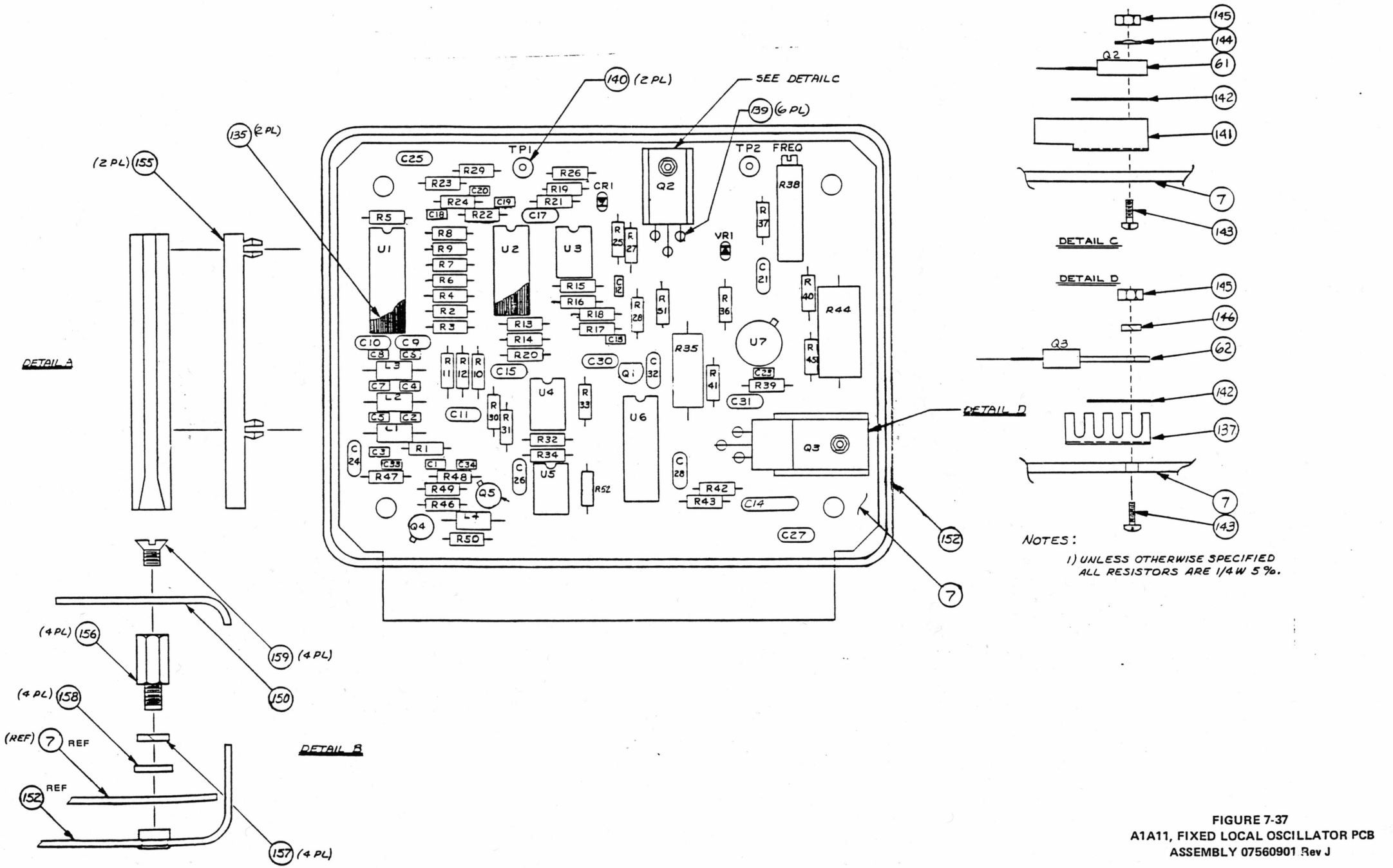
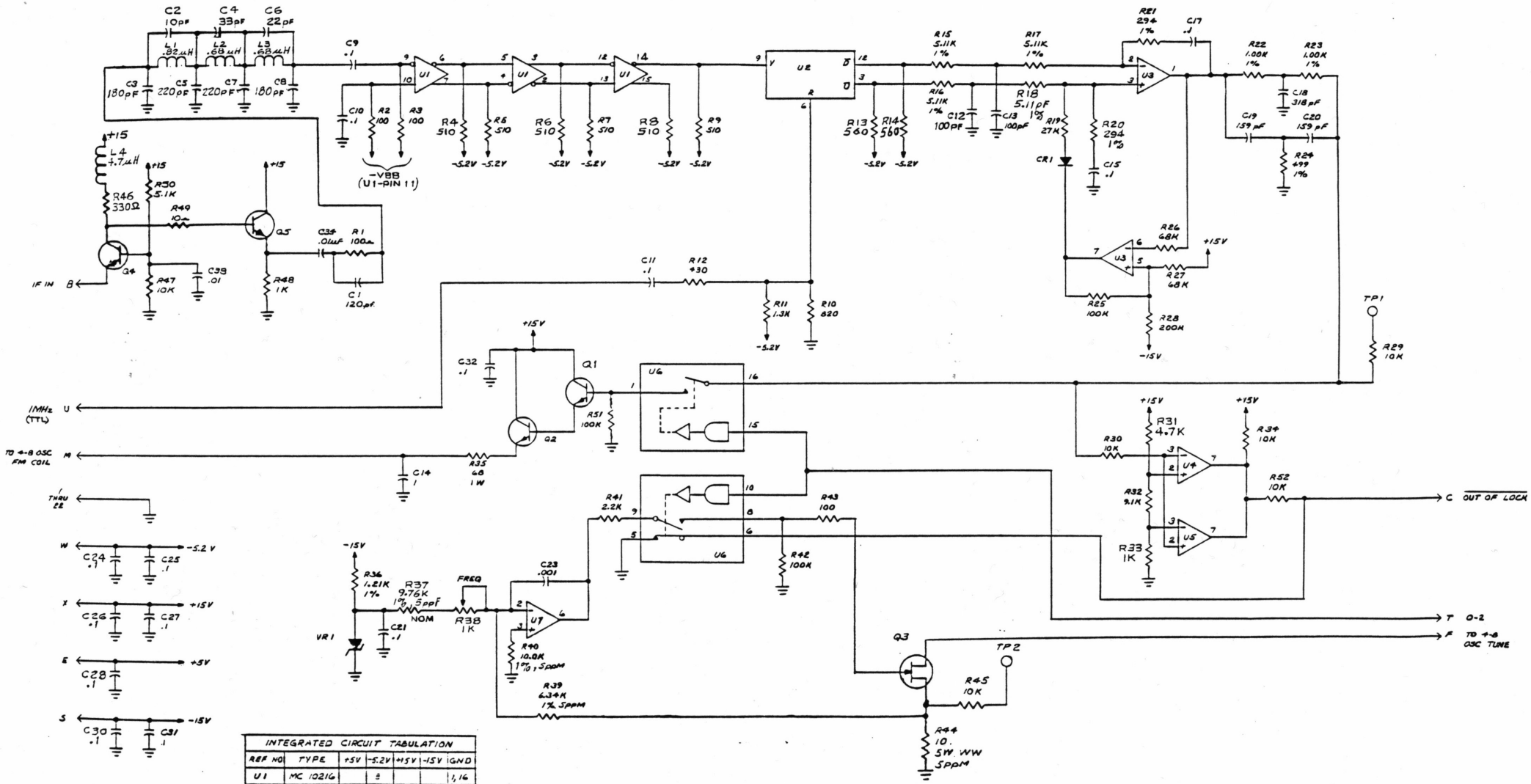


FIGURE 7-37
A1A11, FIXED LOCAL OSCILLATOR PCB
ASSEMBLY 07560901 Rev J



INTEGRATED CIRCUIT TABULATION						
REF NO	TYPE	+5V	-5.2V	+15V	-15V	GND
U1	MC 10216		8			1, 16
U2	MC 12040		7			4, 14
U3	TLO 72			8	4	
U4	SN72311P		1, 4	8		
U5	SN72311P		1, 4	8		
U6	IH5043	12		11	14	13
U7	AD 542			7	4	

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL CAPACITOR VALUES ARE IN μF.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.

FIGURE 7-38
A1A11, FIXED LOCAL OSCILLATOR PCB
SCHEMATIC 7-07560901 Rev E

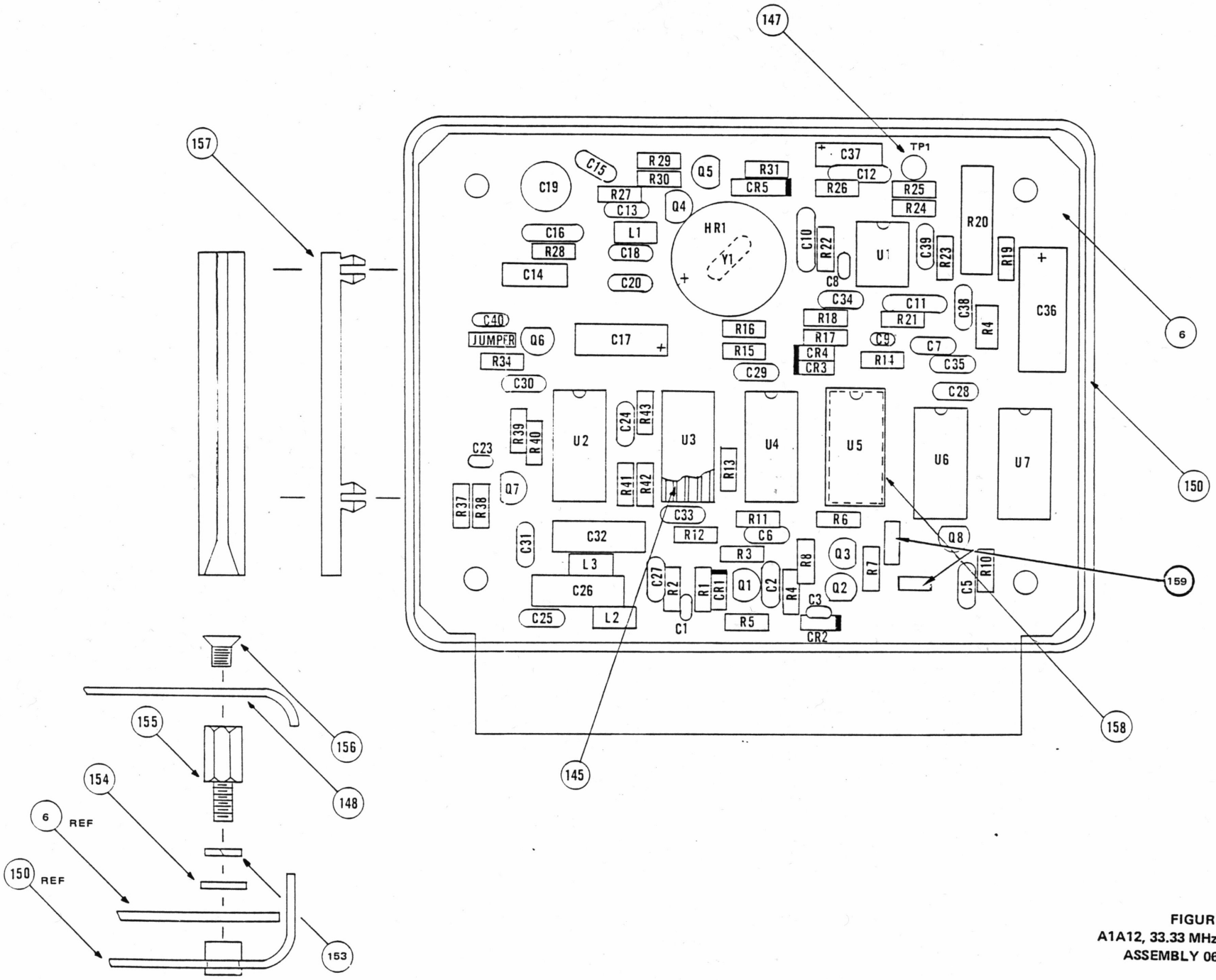
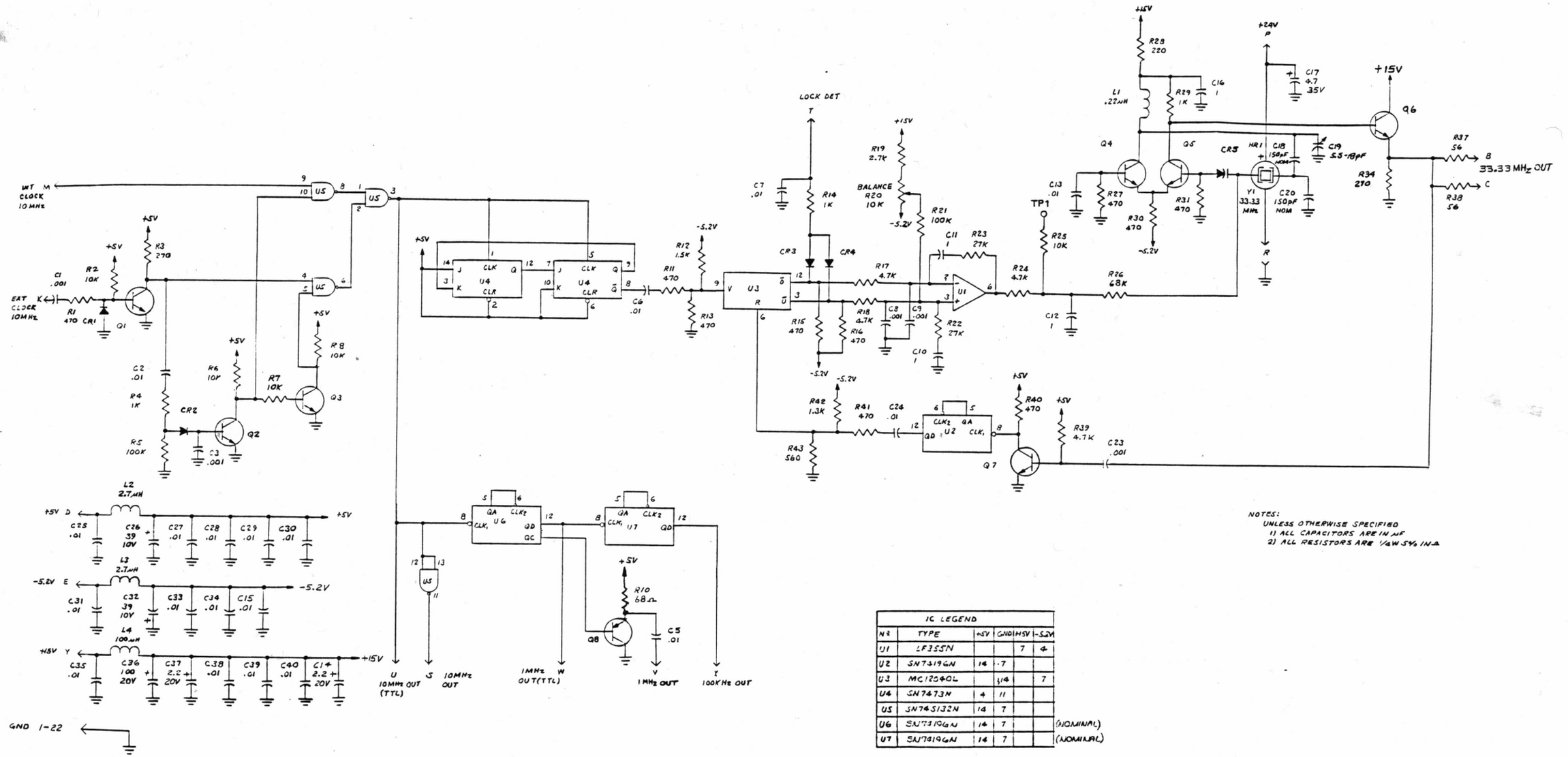


FIGURE 7-39
A1A12, 33.33 MHz REFERENCE PCB
ASSEMBLY 06732401 Rev K



IC LEGEND					
NO	TYPE	+5V	GND	+15V	-5.2V
U1	LF355N			7	4
U2	SN7419GN	14	7		
U3	MC12040L		1/4		7
U4	SN7473N	4	11		
U5	SN74S132N	14	7		
U6	SN7410GN	14	7		(NOMINAL)
U7	SN7419GN	14	7		(NOMINAL)

FIGURE 7-40
A1A12, 33.33 MHz REFERENCE PCB
SCHEMATIC 7-06732401 Rev J

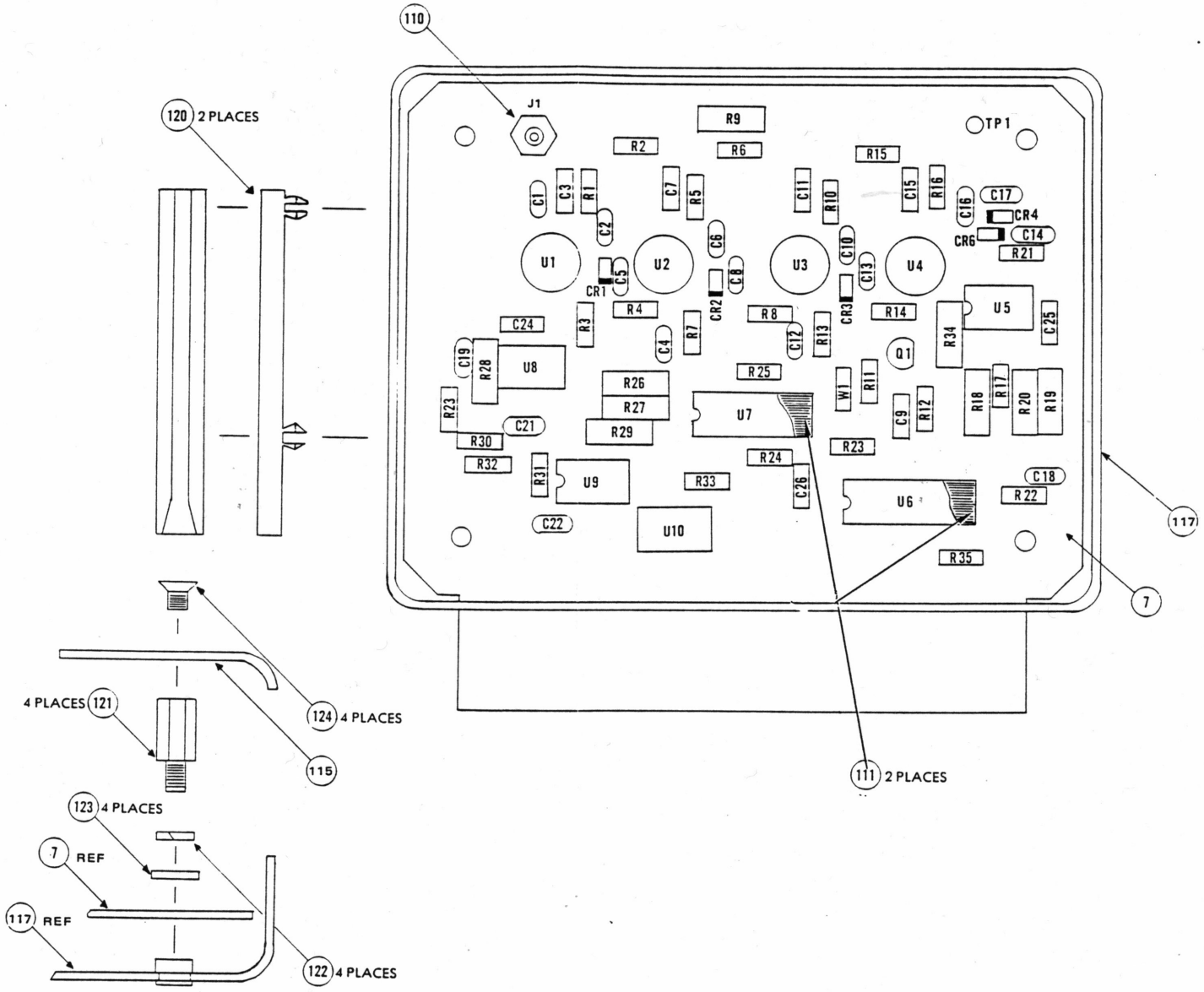
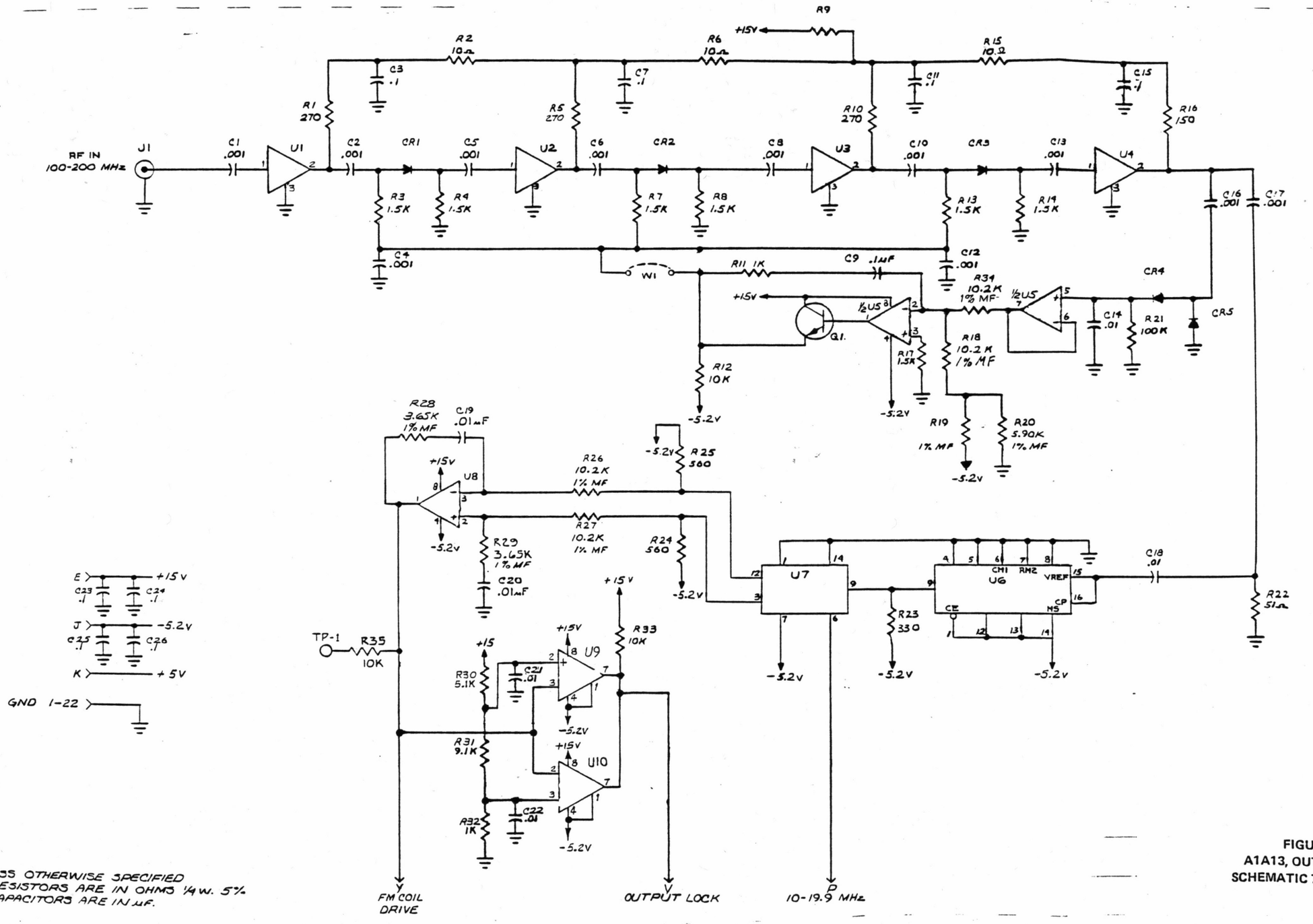


FIGURE 7-41
A1A13, OUTPUT PLL PCB
ASSEMBLY 07538701 Rev E



NOTES: UNLESS OTHERWISE SPECIFIED
1) ALL RESISTORS ARE IN OHMS ¼ W. 5%
2) ALL CAPACITORS ARE IN μF.

FIGURE 7-42
A1A13, OUTPUT PLL PCB
SCHEMATIC 7-07538701 Rev C

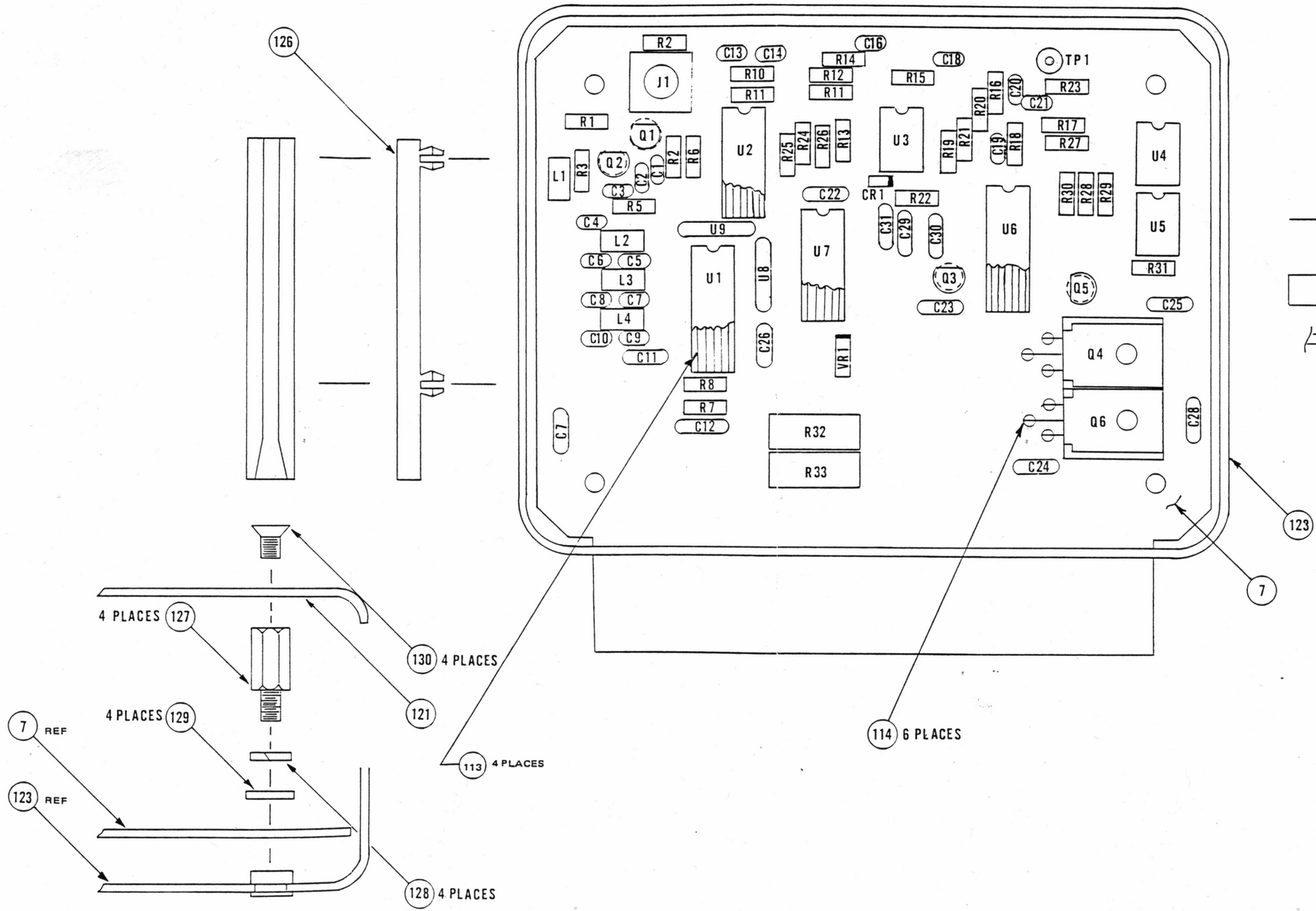
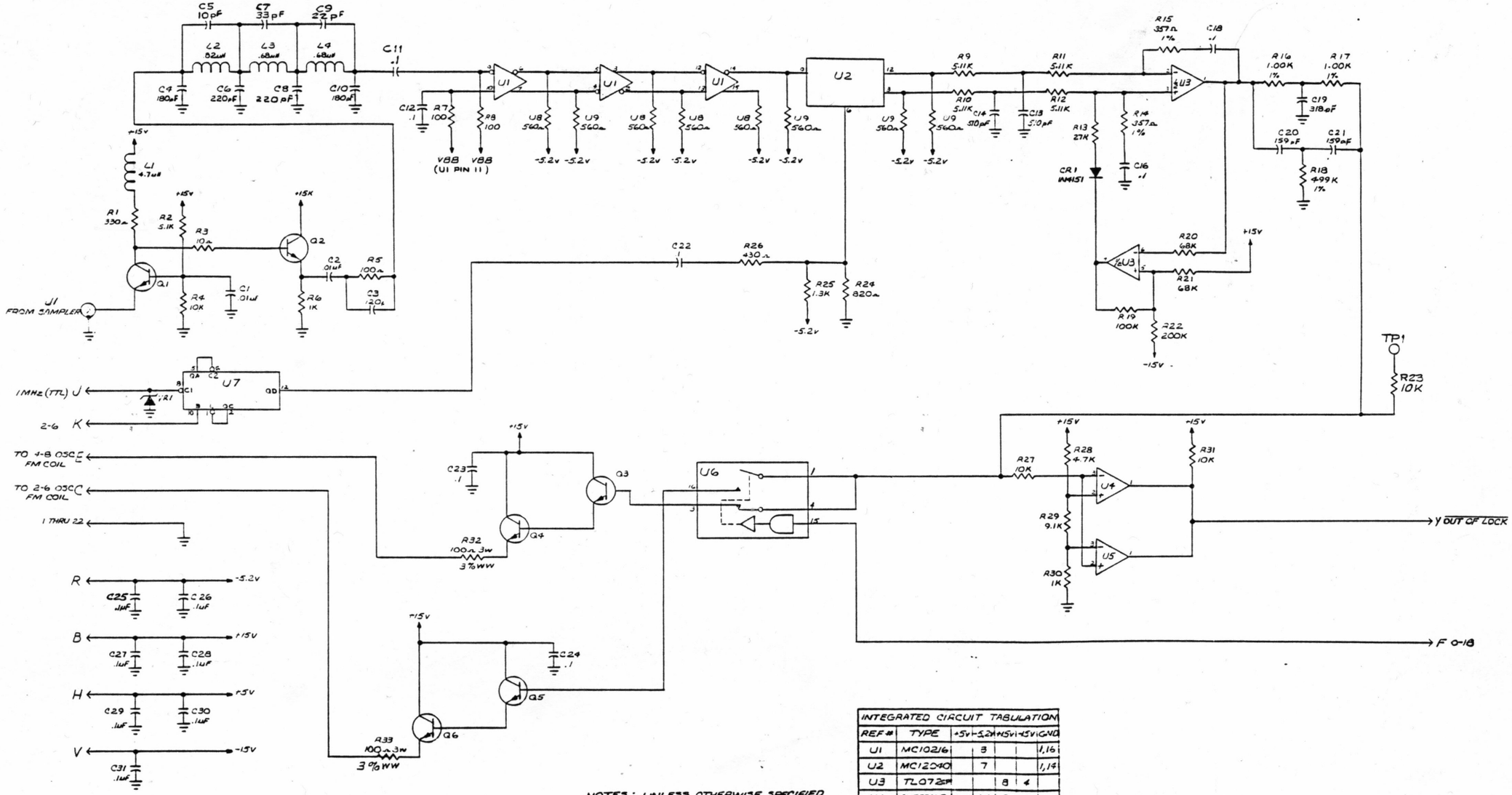


FIGURE 7-43
A1A14, REFERENCE PLL PCB
ASSEMBLY 07561601 Rev D



INTEGRATED CIRCUIT TABULATION						
REF #	TYPE	+5V	-5.2V	+15V	-15V	GND
U1	MC10216		8			1,16
U2	MC12040		7			1,14
U3	TL072CP			8	4	
U4	SN72311P		1,4	8		
U5	SN72311P		1,4	8		
U6	IH5043	12		11	14	13
U7	74LS196	3,4,14				7,11

NOTES: UNLESS OTHERWISE SPECIFIED
1) ALL CAPACITOR VALUES ARE IN μF
2) ALL RESISTOR VALUES ARE IN OHMS 1/4 W 5%

FIGURE 7-44
A1A14, REFERENCE PLL PCB
SCHEMATIC 7-07561601 Rev B

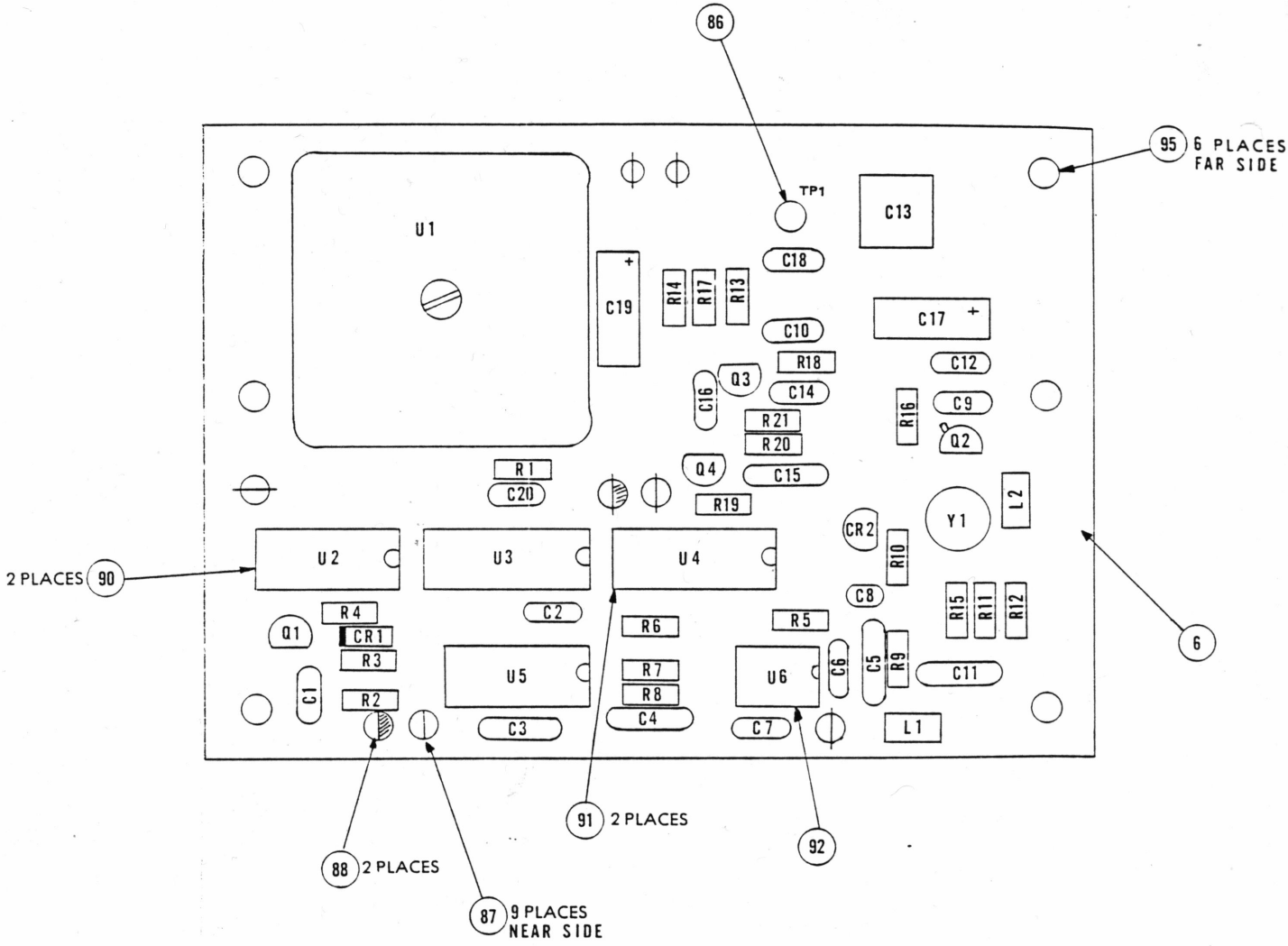
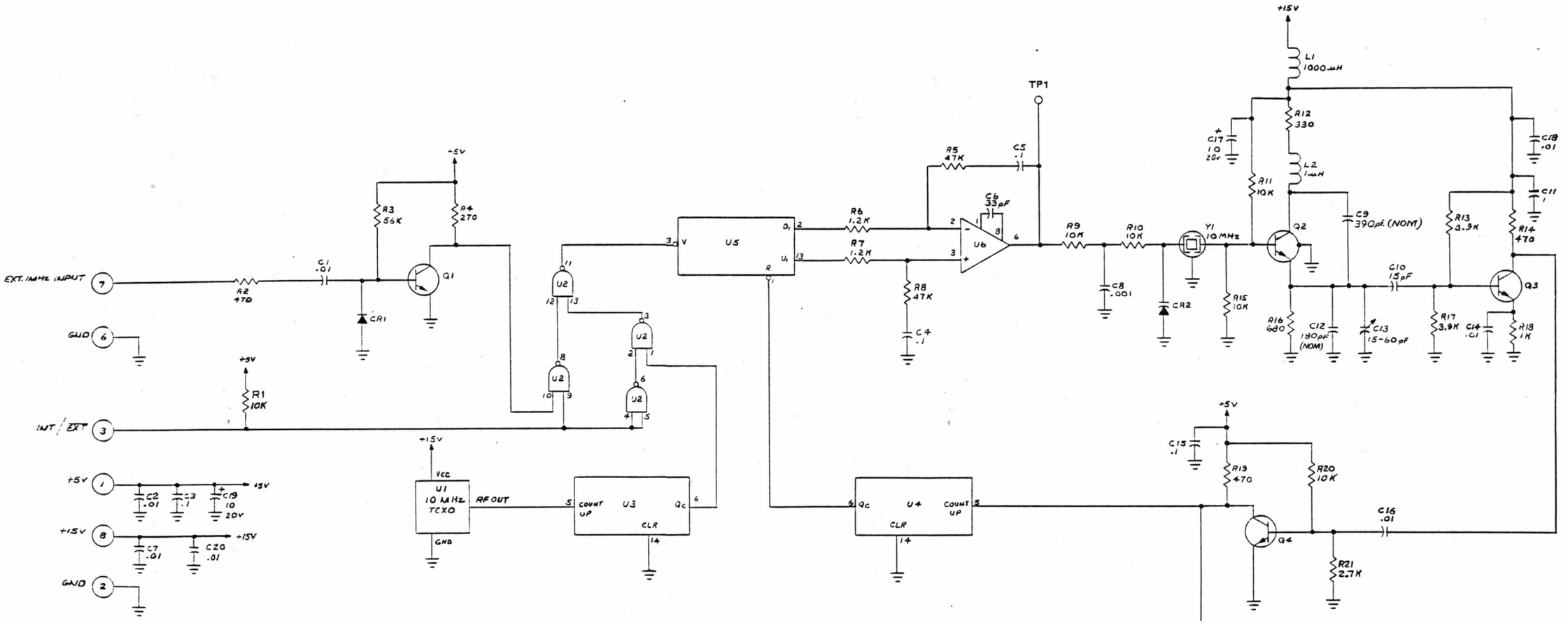


FIGURE 7-45
A1A18, 10 MHz REFERENCE PCB
ASSEMBLY 06733201 Rev K



NOTES: UNLESS OTHERWISE SPECIFIED.
1) ALL RESISTOR VALUES ARE IN OHMS, 1/4 W, 5 %.
2) ALL CAPACITOR VALUES ARE IN µF.

INTEGRATED CIRCUIT TABULATION				
LOC #	TYPE	+5V	+15V	GND
U2	SN 7400N	7		14
U3, U4	SN74LS192N	16		8
U5	MC4044P	7		14
U6	CA 3130E		7	4

FIGURE 7-46
A1A18, 10 MHz REFERENCE PCB
SCHEMATIC 7-06733201 Rev F

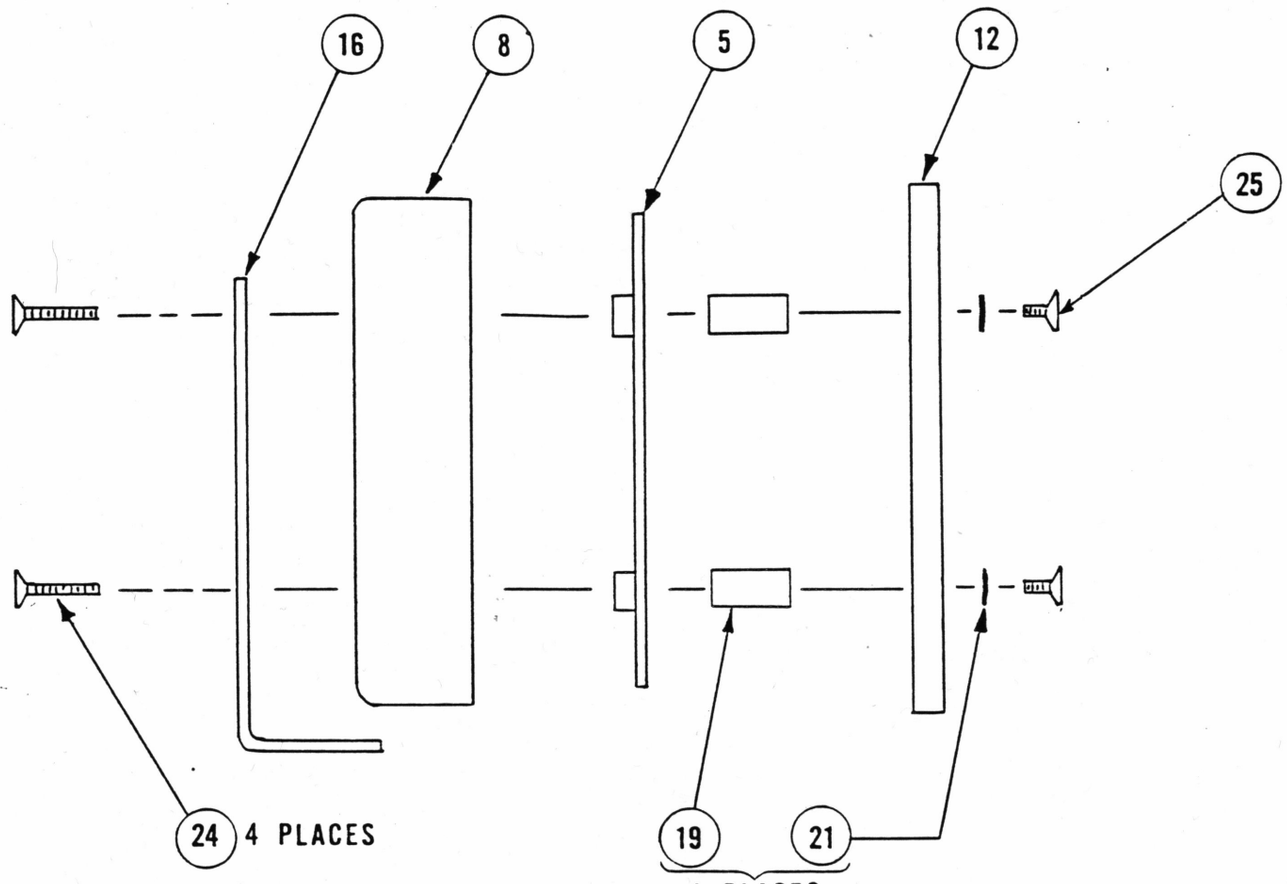


FIGURE 7-47
A1A22, VIDEO AMPLIFIER
ASSEMBLY 06777302 Rev B

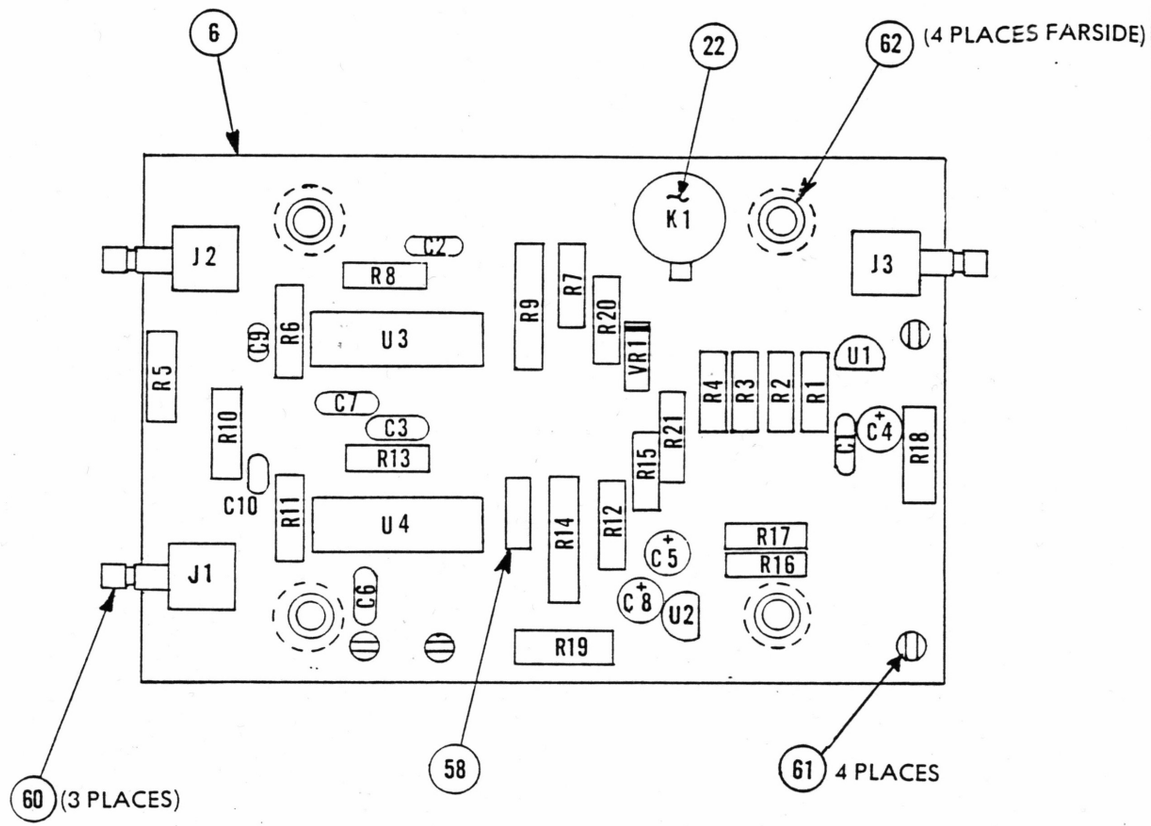
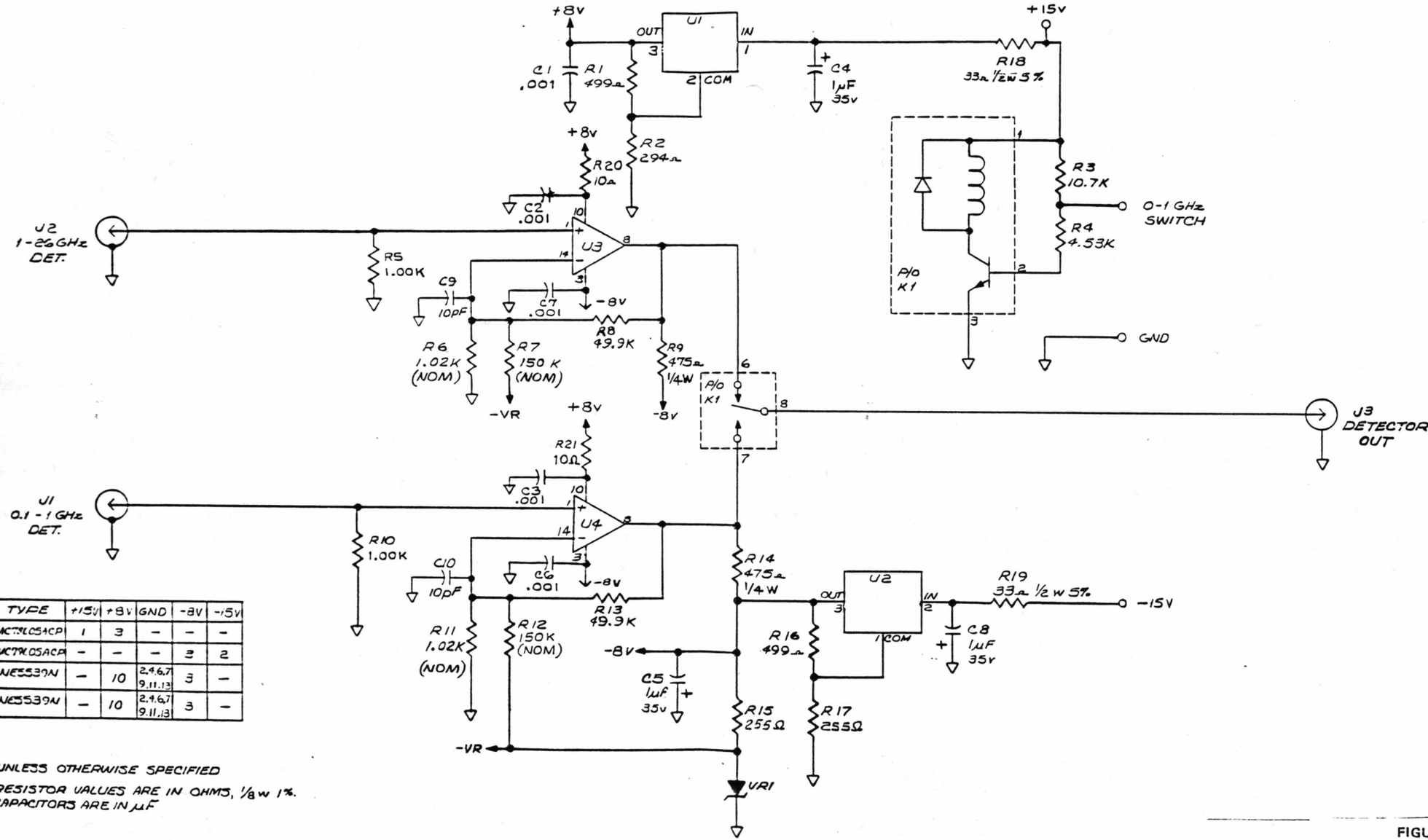


FIGURE 7-48
A1A22A1, VIDEO AMPLIFIER PCB
ASSEMBLY 07570901 Rev C

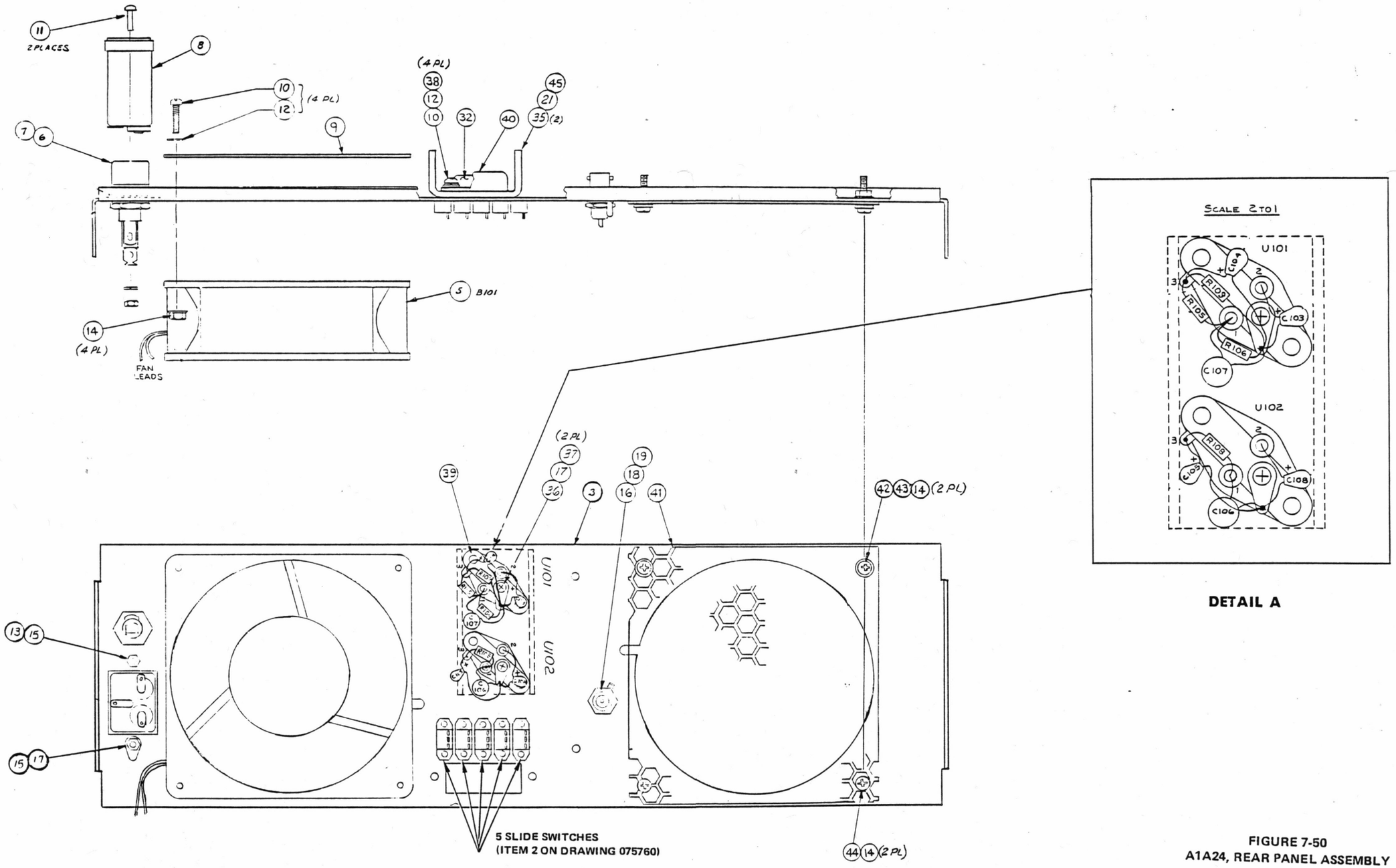


REF	TYPE	+15V	+8V	GND	-8V	-15V
U1	MC78L05ACP	1	3	–	–	–
U2	MC79L05ACP	–	–	–	3	2
U3	NE5539N	–	10	2,4,6,7 9,11,13	3	–
U4	NE5539N	–	10	2,4,6,7 9,11,13	3	–

NOTES: UNLESS OTHERWISE SPECIFIED

1) RESISTOR VALUES ARE IN OHMS, 1/8 W 1%.
2) CAPACITORS ARE IN µF

FIGURE 7-49
A1A22A1, VIDEO AMPLIFIER PCB
SCHEMATIC 7-07570901 Rev C



DETAIL A

FIGURE 7-50
A1A24, REAR PANEL ASSEMBLY
075691 Rev D

NOTES:

1) SEE TEST ASSY 07575101 FOR FULL VIEW OF BOTTOM SIDE IF REQUIRED.

2) FOR THE INSTALLED LOCATION OF EITHER OF ALTERNATE ITEMS 101 (12-18 GHZ OSCILLATOR INSTALLATION, PART NO. 077193) OR 102 (12-18 GHZ OSCILLATOR INSTALLATION, PART NO. 07592802), SEE NOTE 1 ON THE MICROWAVE CHASSIS ASSY DRAWING 07583801. REGARDING THE INTERCHANGEABILITY OF ALTERNATE ITEMS 101 OR 102, NOTE THE FOLLOWING:

   A. EITHER ITEM 101 (PART NO. 077193) OR ITEM 102 (PART NO. 07592802) MAY BE INSTALLED AT THE FACTORY DURING INITIAL EQUIPMENT MANUFACTURE. IF IT IS DESIRED, IN THE FIELD, TO REPLACE A COMPLETE INSTALLATION EITHER INSTALLATION MAY BE USED, REGARDLESS OF WHICH ONE WAS INSTALLED AT THE FACTORY, AS THEY ARE COMPLETELY INTERCHANGEABLE.

   B. IF ONLY A PART OR A SUBASSEMBLY OF AN INSTALLATION IS TO BE FIELD-REPLACED, THE MAINTENANCE PERSONNEL MUST KNOW WHICH OF THE TWO INSTALLATIONS WAS INSTALLED AT THE FACTORY. TO DO THIS, MAINTENANCE PERSONNEL MUST OBTAIN THE PART NO. SHOWN ON THE Y5 OSCILLATOR PIECE-PART. (THERE IS A DIFFERENT Y5 OSCILLATOR IN EACH OF THE TWO INSTALLATIONS.) IF THE Y5 OSCILLATOR PIECE-PART IS PART NO. 11690801, ITEM 101 WAS INSTALLED AT THE FACTORY. IF THE Y5 OSCILLATOR PIECE-PART IS PART NO. 11772002, ITEM 102 WAS INSTALLED AT THE FACTORY.

3) FOR THE INSTALLED LOCATION OF EITHER OF ALTERNATE ITEMS 103 (8-12 AND 18-26 GHZ OSCILLATOR INSTALLATION, PART NO. 06764402) OR 104 (8-12 AND 18-26 GHZ OSCILLATOR INSTALLATION, PART NO. 07592801), SEE NOTE 2 ON THE MICROWAVE CHASSIS ASSY DRAWING 07583801. REGARDING THE INTERCHANGEABILITY OF ALTERNATE ITEMS 103 OR 104, NOTE THE FOLLOWING:

   A. EITHER ITEM 103 (PART NO. 06764402) OR ITEM 104 (PART NO. 07592801) MAY BE INSTALLED AT THE FACTORY DURING INITIAL EQUIPMENT MANUFACTURE. IF IT IS DESIRED, IN THE FIELD, TO REPLACE A COMPLETE INSTALLATION EITHER INSTALLATION MAY BE USED, REGARDLESS OF WHICH ONE WAS INSTALLED AT THE FACTORY, AS THEY ARE COMPLETELY INTERCHANGEABLE.

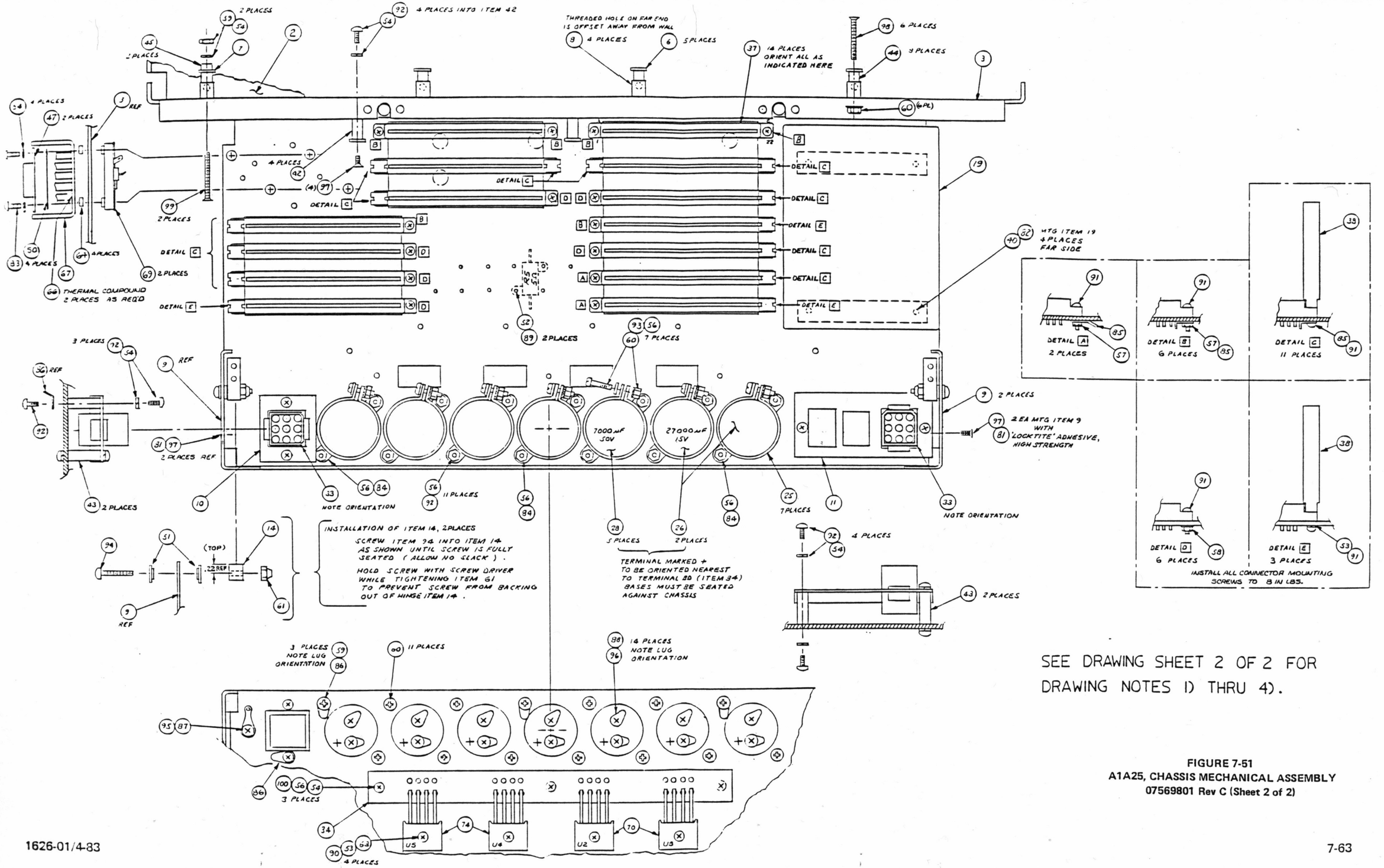
   B. IF ONLY A PART OR A SUBASSEMBLY OF AN INSTALLATION IS TO BE FIELD-REPLACED, THE MAINTENANCE PERSONNEL MUST KNOW WHICH OF THE TWO INSTALLATIONS WAS INSTALLED AT THE FACTORY. TO DO THIS, MAINTENANCE PERSONNEL MUST OBTAIN THE PART NO. SHOWN ON THE Y4 OSCILLATOR PIECE-PART. (THERE IS A DIFFERENT Y4 OSCILLATOR IN EACH OF THE TWO INSTALLATIONS WHEREAS THE PIECE-PART NO. OF THE Y6 OSCILLATOR (PART NO. 117834) IS THE SAME IN BOTH INSTALLATIONS.) IF THE Y4 OSCILLATOR PIECE-PART IS PART NO. 11691001, ITEM 103 WAS INSTALLED AT THE FACTORY. IF THE Y4 OSCILLATOR PIECE-PART IS PART NO. 11771902, ITEM 104 WAS INSTALLED AT THE FACTORY.

4) FOR THE INSTALLED LOCATION OF EITHER OF ALTERNATE ITEMS 105 (ATTENUATOR BRACKET ASSY AND COUPLER BRACKET ASSY INSTALLATION, PART NO. 077199) OR 106 (ATTENUATOR BRACKET ASSY AND COUPLER BRACKET ASSY INSTALLATION, PART NO. 077200), SEE NOTES 3 AND 4 ON THE MICROWAVE CHASSIS ASSY DRAWING 07583801. REGARDING THE INTERCHANGEABILITY OF ALTERNATE ITEMS 105 OR 106, NOTE THE FOLLOWING:

   A. EITHER ITEM 105 (PART NO. 077199) OR ITEM 106 (PART NO. 077200) MAY BE INSTALLED AT THE FACTORY DURING INITIAL EQUIPMENT MANUFACTURE. IF IT IS DESIRED, IN THE FIELD, TO REPLACE A COMPLETE INSTALLATION EITHER INSTALLATION MAY BE USED, REGARDLESS OF WHICH ONE WAS INSTALLED AT THE FACTORY, AS THEY ARE COMPLETELY INTERCHANGEABLE.

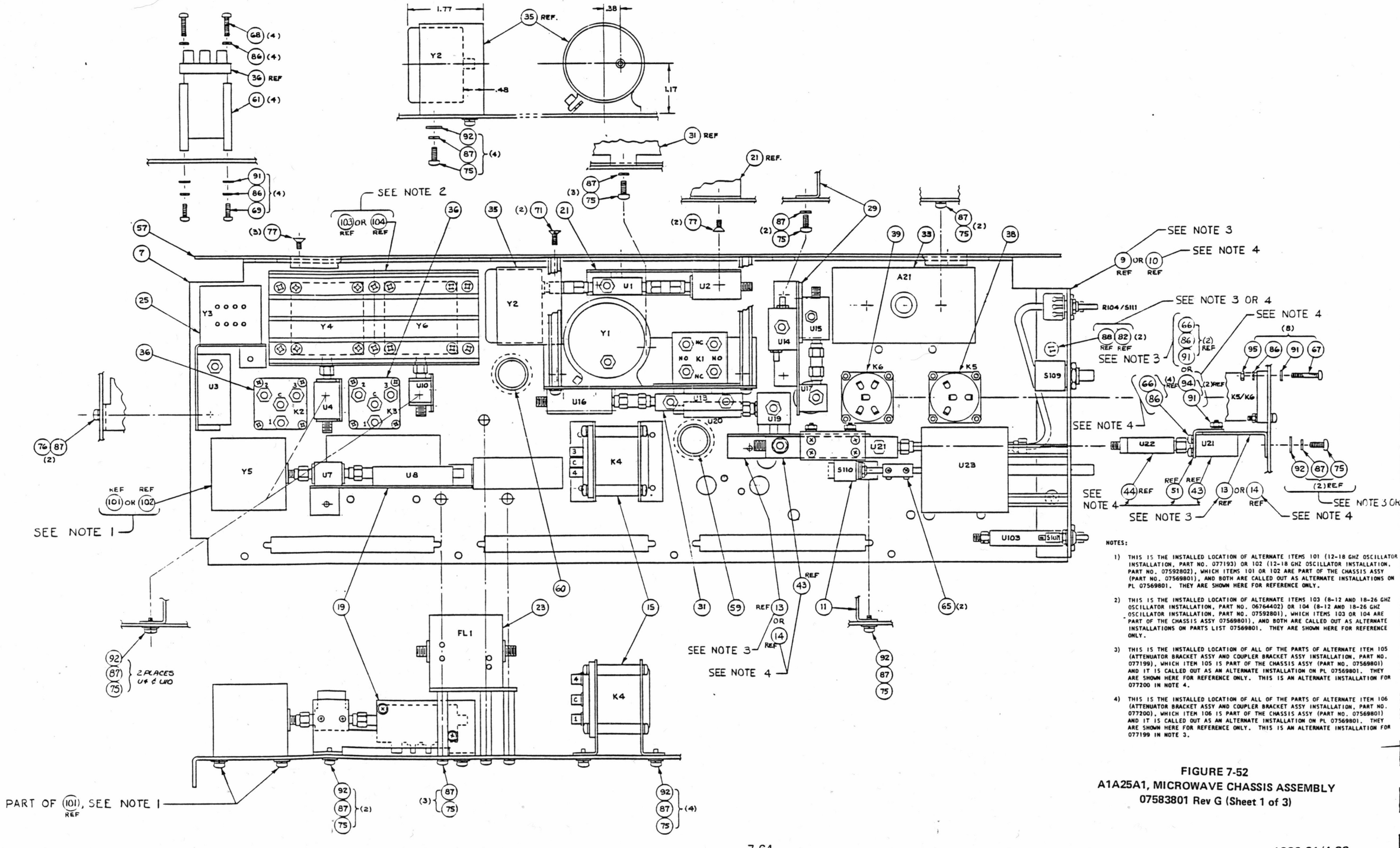
   B. IF ONLY A PART OR A SUBASSEMBLY OF AN INSTALLATION IS TO BE FIELD-REPLACED, THE MAINTENANCE PERSONNEL MUST KNOW WHICH OF THE TWO INSTALLATIONS WAS INSTALLED AT THE FACTORY AND THEN MUST ORDER ONLY PARTS OR SUBASSEMBLIES THAT ARE USED BY THE FACTORY TO MAKE UP ONLY THAT INSTALLATION. TO DO THIS, MAINTENANCE PERSONNEL MUST OBTAIN THE PART NO. SHOWN ON THE U19 COUPLER PIECE-PART. (THERE IS A DIFFERENT U19 COUPLER IN EACH OF THE TWO INSTALLATIONS.) IF THE U19 COUPLER PIECE-PART IS PART NO. 117715, ITEM 105 WAS INSTALLED AT THE FACTORY. IF THE U19 COUPLER PIECE-PART IS PART NO. 11771501, ITEM 106 WAS INSTALLED AT THE FACTORY.

FIGURE 7-51
A1A25, CHASSIS MECHANICAL ASSEMBLY
07569801 Rev C (Sheet 1 of 2)



SEE DRAWING SHEET 2 OF 2 FOR DRAWING NOTES 1) THRU 4).

FIGURE 7-51
A1A25, CHASSIS MECHANICAL ASSEMBLY
07569801 Rev C (Sheet 2 of 2)



NOTES:

1) THIS IS THE INSTALLED LOCATION OF ALTERNATE ITEMS 101 (12-18 GHZ OSCILLATOR INSTALLATION, PART NO. 077193) OR 102 (12-18 GHZ OSCILLATOR INSTALLATION, PART NO. 07592802), WHICH ITEMS 101 OR 102 ARE PART OF THE CHASSIS ASSY (PART NO. 07569801), AND BOTH ARE CALLED OUT AS ALTERNATE INSTALLATIONS ON PL 07569801. THEY ARE SHOWN HERE FOR REFERENCE ONLY.

2) THIS IS THE INSTALLED LOCATION OF ALTERNATE ITEMS 103 (8-12 AND 18-26 GHZ OSCILLATOR INSTALLATION, PART NO. 06764402) OR 104 (8-12 AND 18-26 GHZ OSCILLATOR INSTALLATION, PART NO. 07592801), WHICH ITEMS 103 OR 104 ARE PART OF THE CHASSIS ASSY 07569801, AND BOTH ARE CALLED OUT AS ALTERNATE INSTALLATIONS ON PARTS LIST 07569801. THEY ARE SHOWN HERE FOR REFERENCE ONLY.

3) THIS IS THE INSTALLED LOCATION OF ALL OF THE PARTS OF ALTERNATE ITEM 105 (ATTENUATOR BRACKET ASSY AND COUPLER BRACKET ASSY INSTALLATION, PART NO. 077199), WHICH ITEM 105 IS PART OF THE CHASSIS ASSY (PART NO. 07569801) AND IT IS CALLED OUT AS AN ALTERNATE INSTALLATION ON PL 07569801. THEY ARE SHOWN HERE FOR REFERENCE ONLY. THIS IS AN ALTERNATE INSTALLATION FOR 077200 IN NOTE 4.

4) THIS IS THE INSTALLED LOCATION OF ALL OF THE PARTS OF ALTERNATE ITEM 106 (ATTENUATOR BRACKET ASSY AND COUPLER BRACKET ASSY INSTALLATION, PART NO. 077200), WHICH ITEM 106 IS PART OF THE CHASSIS ASSY (PART NO. 07569801) AND IT IS CALLED OUT AS AN ALTERNATE INSTALLATION ON PL 07569801. THEY ARE SHOWN HERE FOR REFERENCE ONLY. THIS IS AN ALTERNATE INSTALLATION FOR 077199 IN NOTE 3.

FIGURE 7-52
A1A25A1, MICROWAVE CHASSIS ASSEMBLY
07583801 Rev G (Sheet 1 of 3)

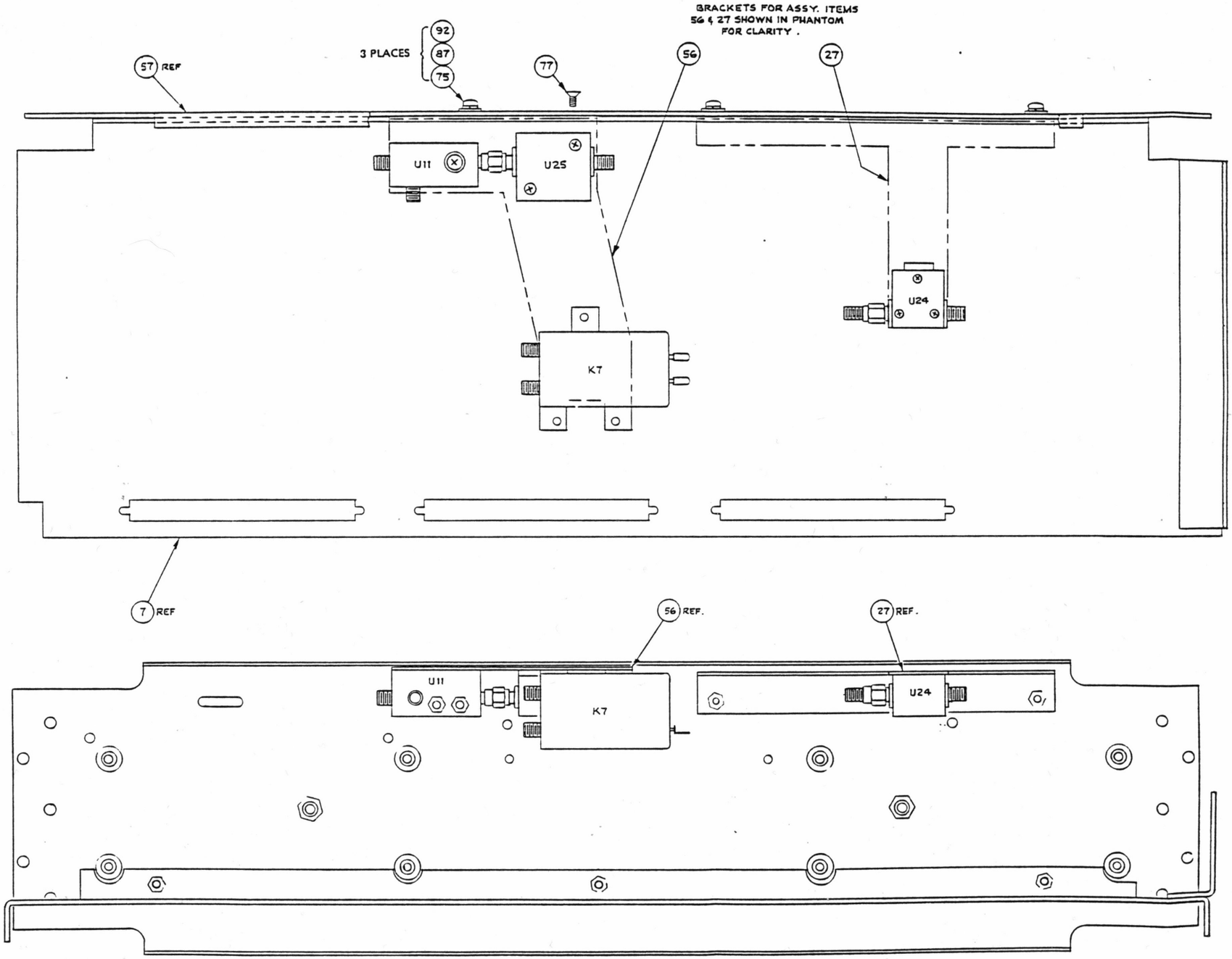


FIGURE 7-52
A1A25A1, MICROWAVE CHASSIS ASSEMBLY
07583801 Rev G (Sheet 2 of 3)

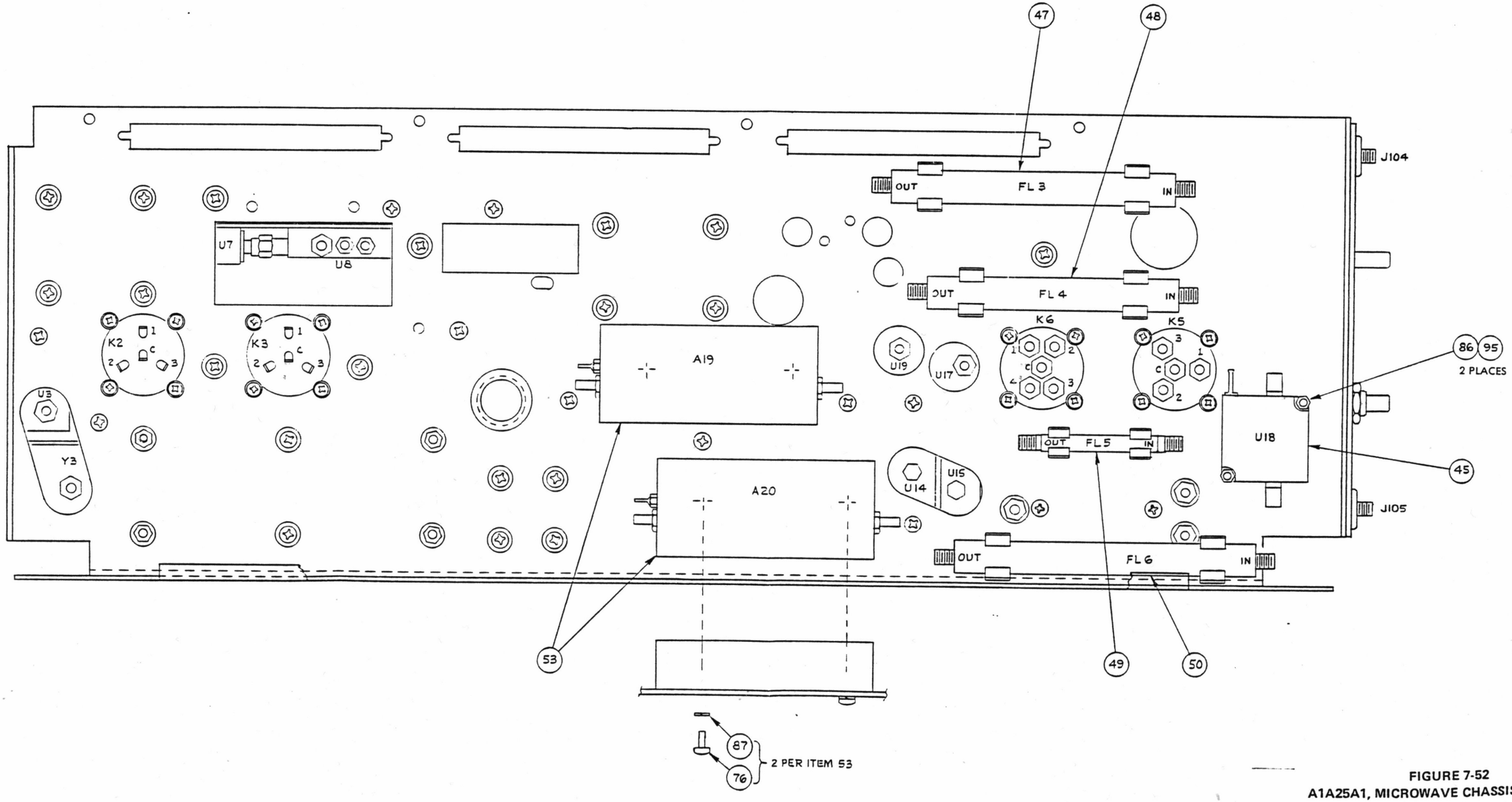


FIGURE 7-52
A1A25A1, MICROWAVE CHASSIS ASSEMBLY
07583801 Rev G (Sheet 3 of 3)

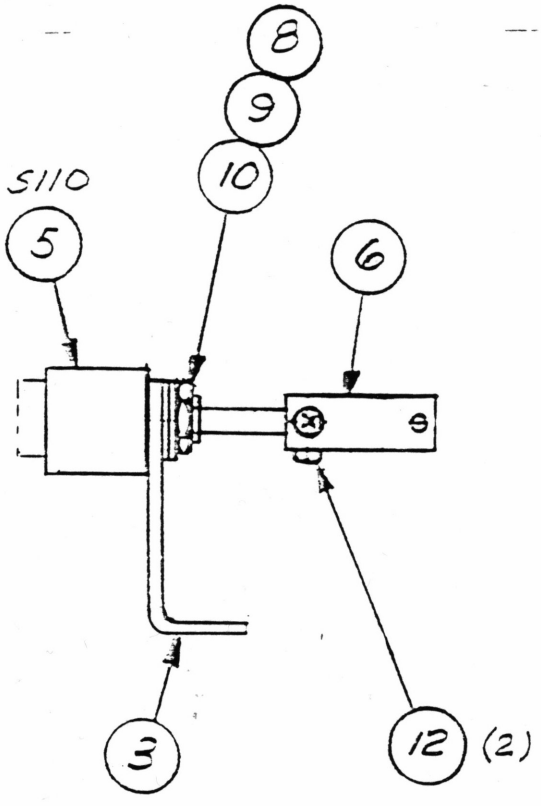
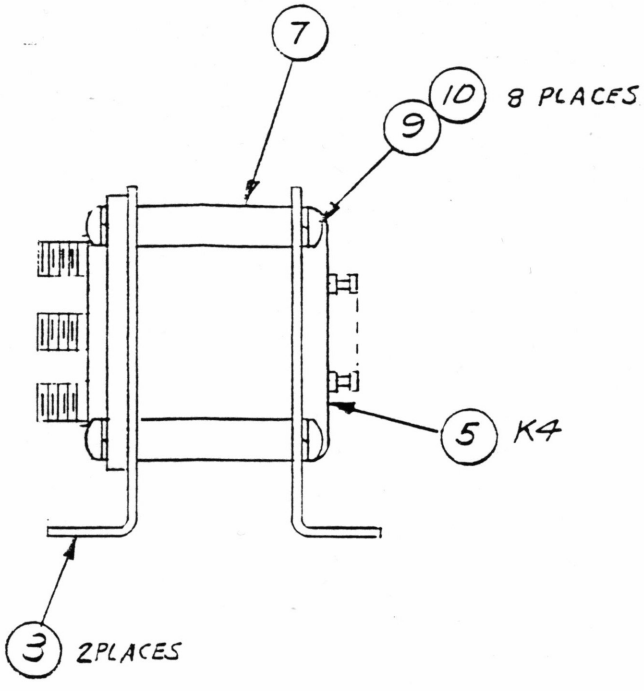


FIGURE 7-53
A1A25A1A3, SWITCH BRACKET
ASSEMBLY 06735002 Rev B



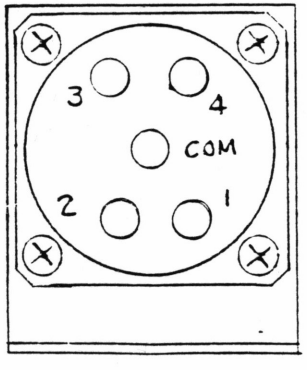


FIGURE 7-54
A1A25A1A5, OUTPUT RELAY BRACKET
ASSEMBLY 06764302 Rev A

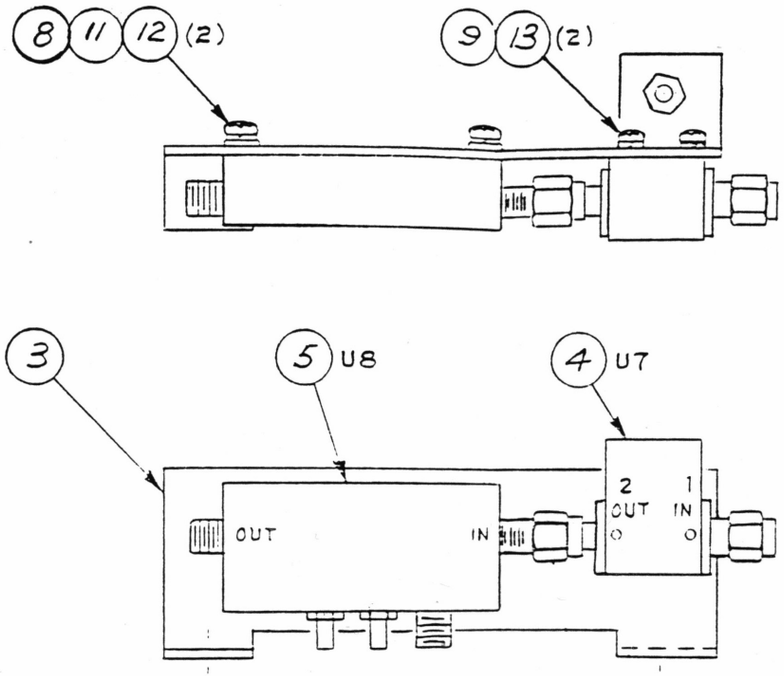


FIGURE 7-55
A1A25A1A7, 12 to 18 GHz MODULE BRACKET
ASSEMBLY 07581201 Rev B

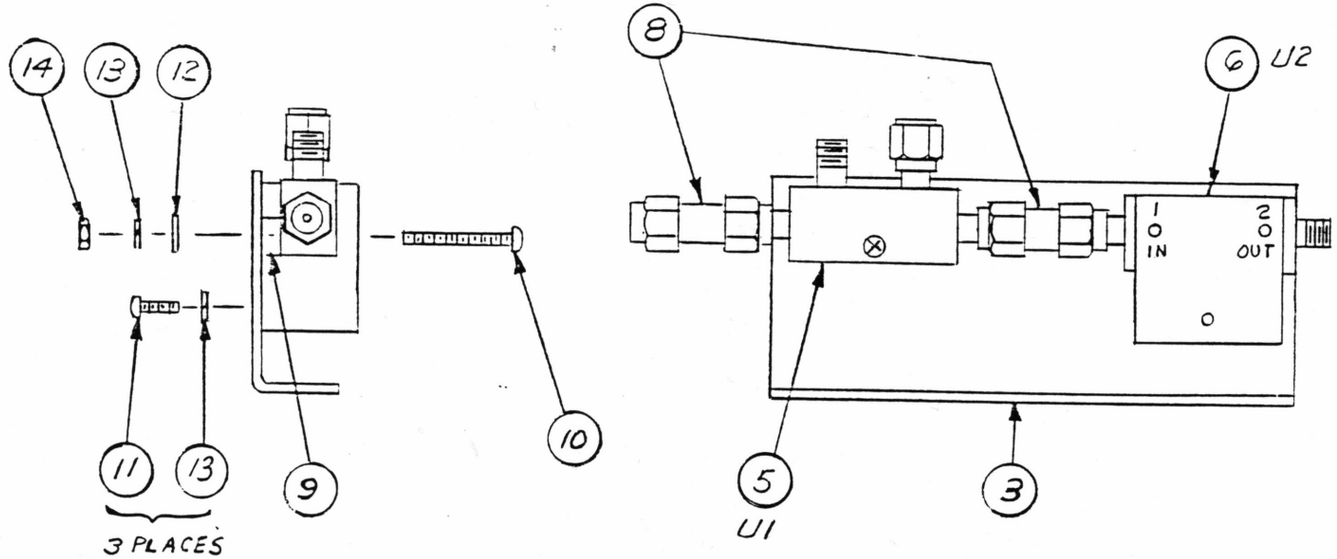


FIGURE 7-56
A1A25A1A8, 4 to 8 GHz BRACKET
ASSEMBLY 06779302 Rev A

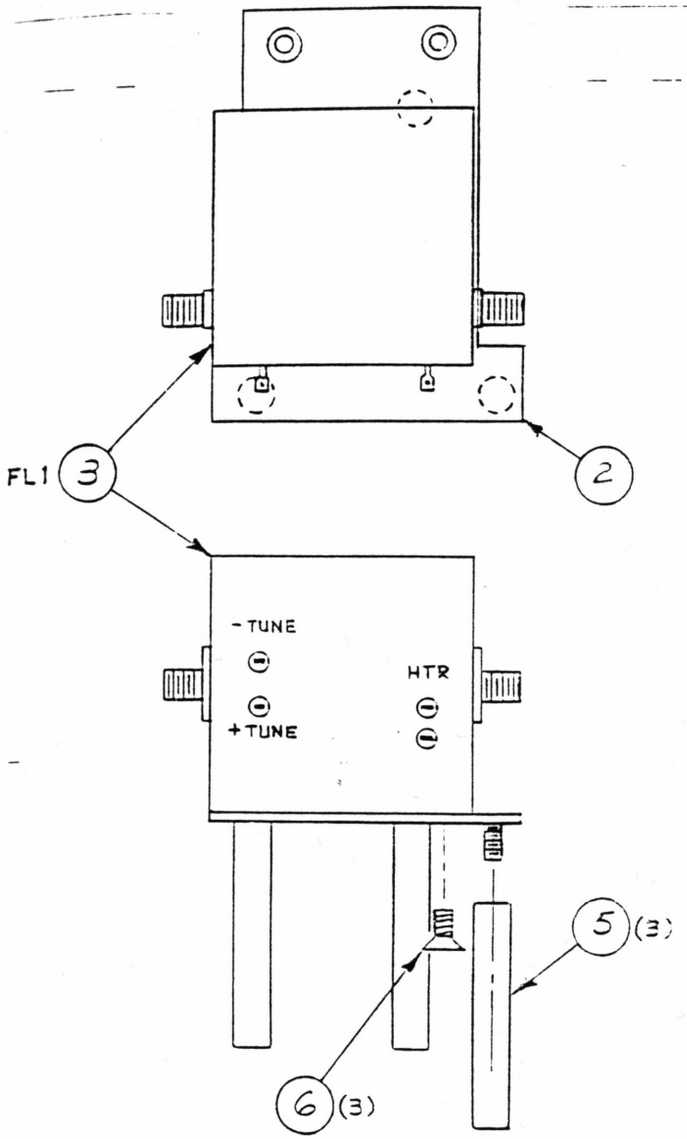


FIGURE 7-57
A1A25A1A9, YIG FILTER BASE
ASSEMBLY 07581701 Rev B

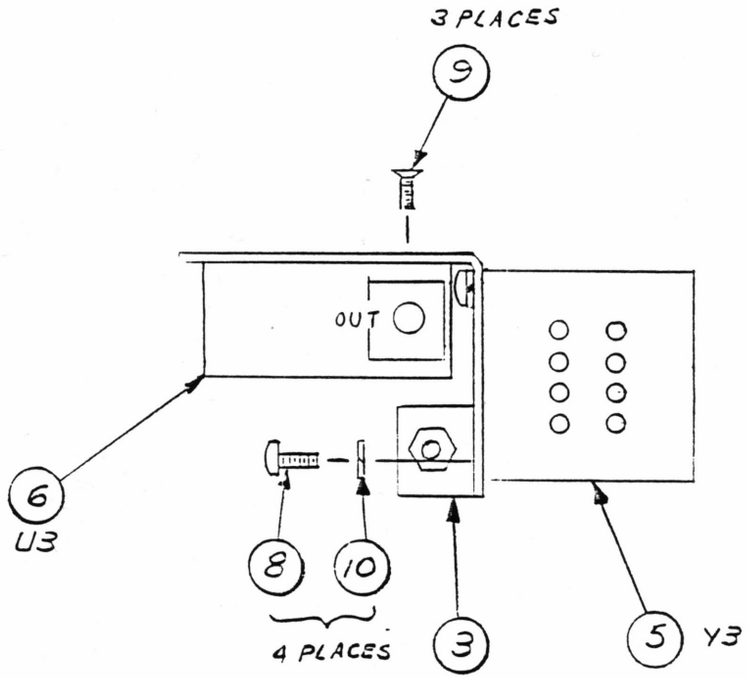


FIGURE 7-58
A1A25A1A10, 2 to 4 GHz BRACKET
ASSEMBLY 06779002 Rev A

NOTES:

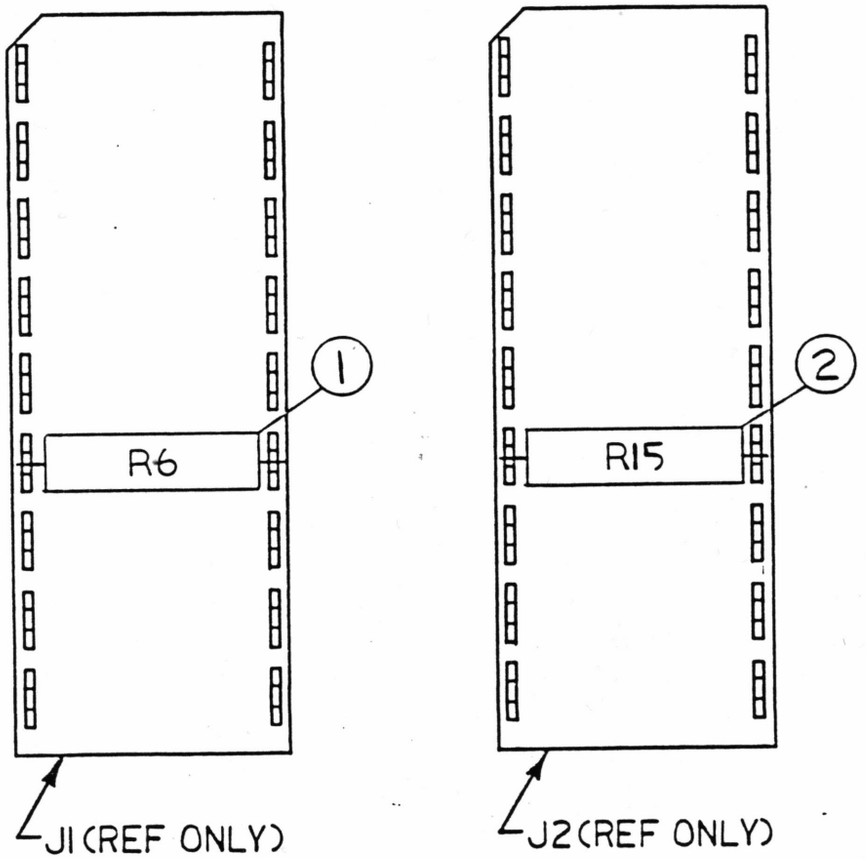
1. ALL RESISTORS IN THIS KIT ARE FACTORY-SELECTED TO ELECTRONICALLY MATCH THE OSCILLATOR IN THIS KIT PRIOR TO THIS KIT BEING FACTORY-INSTALLED IN THE INSTRUMENT. ONLY THE "NOMINAL VALUES", AND NOMINAL VALUE PART NUMBERS, ARE SHOWN ON THE PARTS LIST. THE VALUE OF A RESISTOR IN ANY ACTUAL KIT MAY DIFFER FROM THE "NOMINAL VALUE" SHOWN ON THE PARTS LIST, AND MAY DIFFER BETWEEN KITS OF THIS SAME PART NUMBER. ALL RESISTORS ARE "FIXED, METAL FILM" AND, UNLESS OTHERWISE NOTED ON THE PARTS LIST AND NEXT TO THE DRAWING CALLOUT, ALL RESISTORS ARE "1/10 WATT, ±25 PPM/DEG C" AND ARE FACTORY-SELECTED FROM MILITARY TYPE RN55E____F. FOR FIELD-REPLACEMENT OR FIELD-REPAIR OF THIS KIT, SEE "A" AND "B", BELOW.

   A. IF THE OSCILLATOR FAILS IN THE FIELD, A COMPLETE NEW KIT MUST BE FIELD-INSTALLED AFTER FIRST REMOVING FROM THE INSTRUMENT THE FAILED OSCILLATOR AND ALL RESISTORS THAT ARE PART OF THE KIT. (IT MAY BE NOTED THAT THE RESISTANCE VALUE OF A RESISTOR IN THE NEW KIT MAY BE DIFFERENT THAN THE RESISTANCE VALUE OF THE RESISTOR THAT IT IS REPLACING IN THE INSTRUMENT. THE REASON FOR THIS POSSIBLE DIFFERENCE IS DUE TO THE FACTORY-SELECTIONS MENTIONED ABOVE, AND THE RESISTOR IN THE NEW KIT MUST BE USED.)

   B. IF A RESISTOR FAILS IN THE FIELD, IT CAN BE FIELD-REPLACED BUT ONLY WITH AN EXACT DUPLICATE OF THE ONE IN THE INSTRUMENT. TO ACCOMPLISH THIS, MAINTENANCE PERSONNEL MUST BE ABLE TO IDENTIFY THE EXACT RESISTANCE VALUE OF THE FAILED RESISTOR IN THE INSTRUMENT. IF THE EXACT RESISTANCE VALUE OF THE FAILED RESISTOR CAN NOT BE DETERMINED, A COMPLETE NEW KIT MUST BE FIELD-INSTALLED AS IN "A", ABOVE.

2. RESISTORS R6 AND R15 (ITEMS 1 AND 2) ARE INSTALLED WHERE SHOWN IN J1 AND J2 (ITEMS 250 AND 251 ON ASSY DRAWING 07559601).

3. FOR INSTALLED LOCATION OF ITEM 3 (Y3), SEE CALLOUT 5 ON ASSY DRAWING 06779002.



SEE SEPARATE PARTS LIST

FIGURE 7-59
A1A25A1A10A1, 2 to 4 GHz OSCILLATOR KIT
077192 Rev A

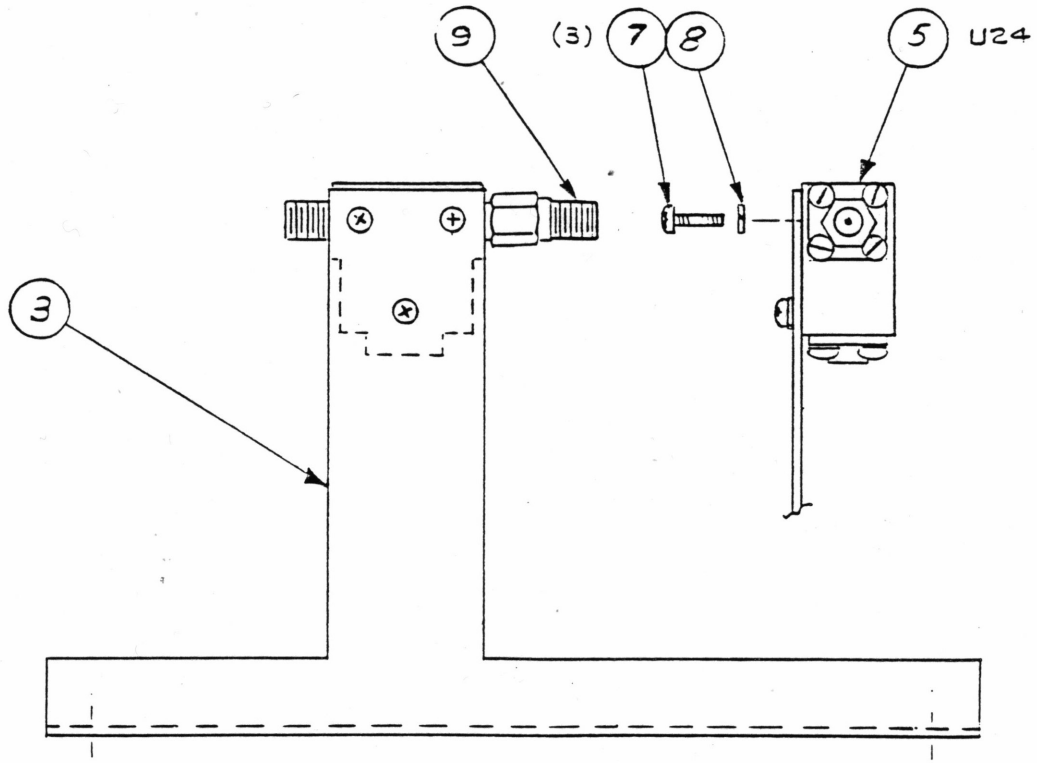


FIGURE 7-60
A1A25A1A11, ISOLATOR BRACKET
ASSEMBLY 07581301 Rev B

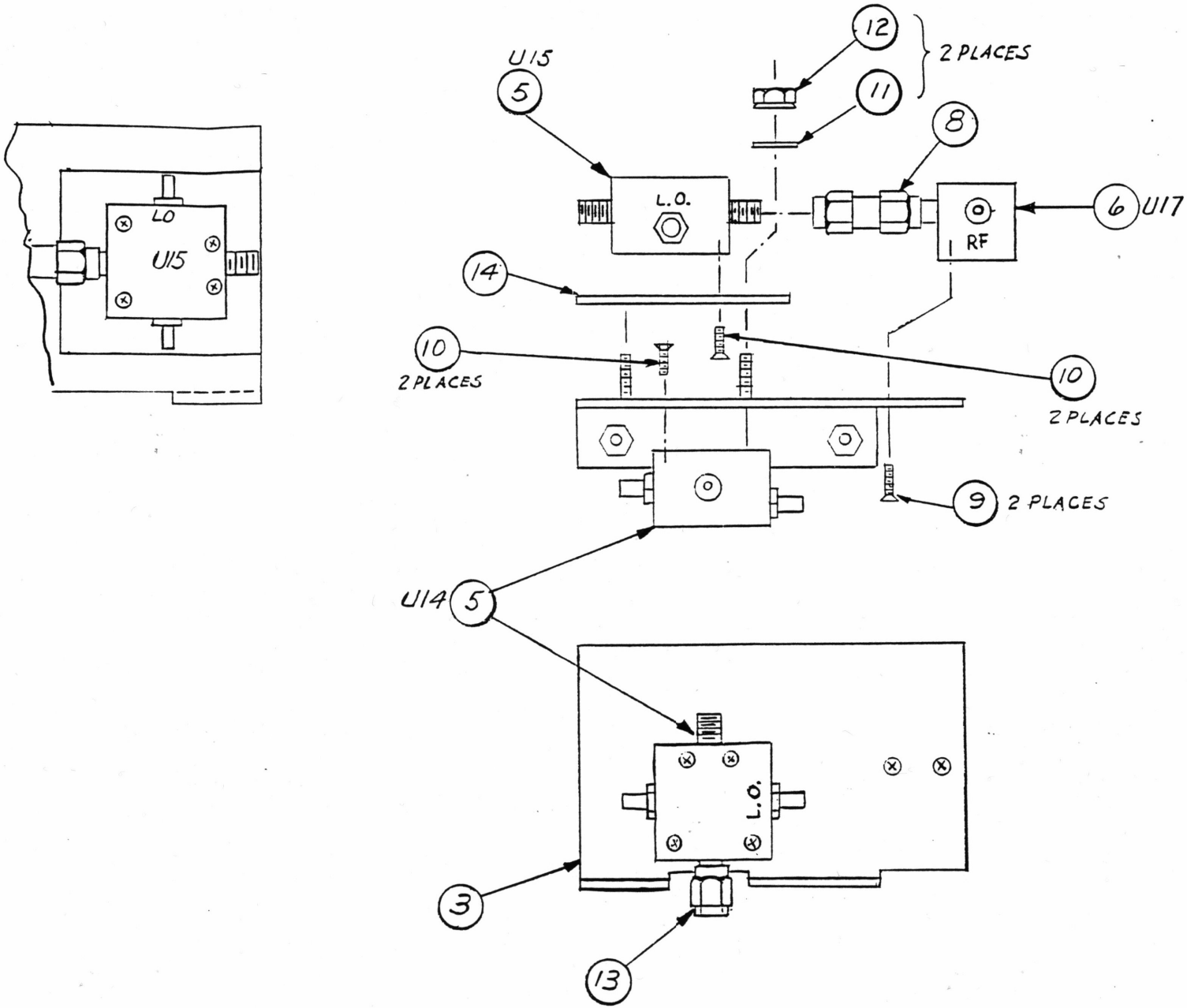


FIGURE 7-61
A1A25A1A12, SAMPLER BRACKET
ASSEMBLY 06764102 Rev A

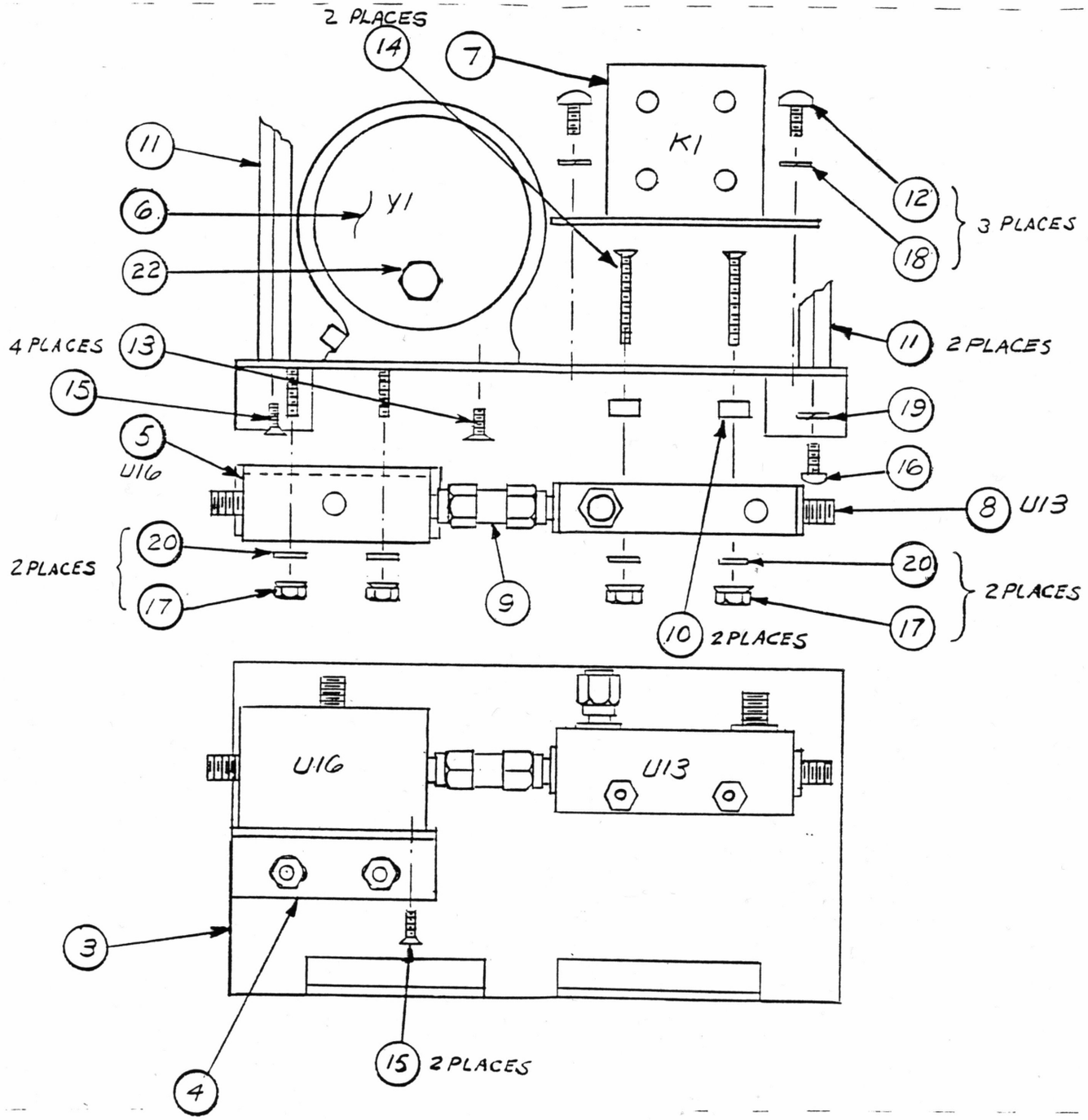


FIGURE 7-62
A1A25A1A13, 1.9 to 6 GHz BRACKET
ASSEMBLY 07516202 Rev A

NOTES:

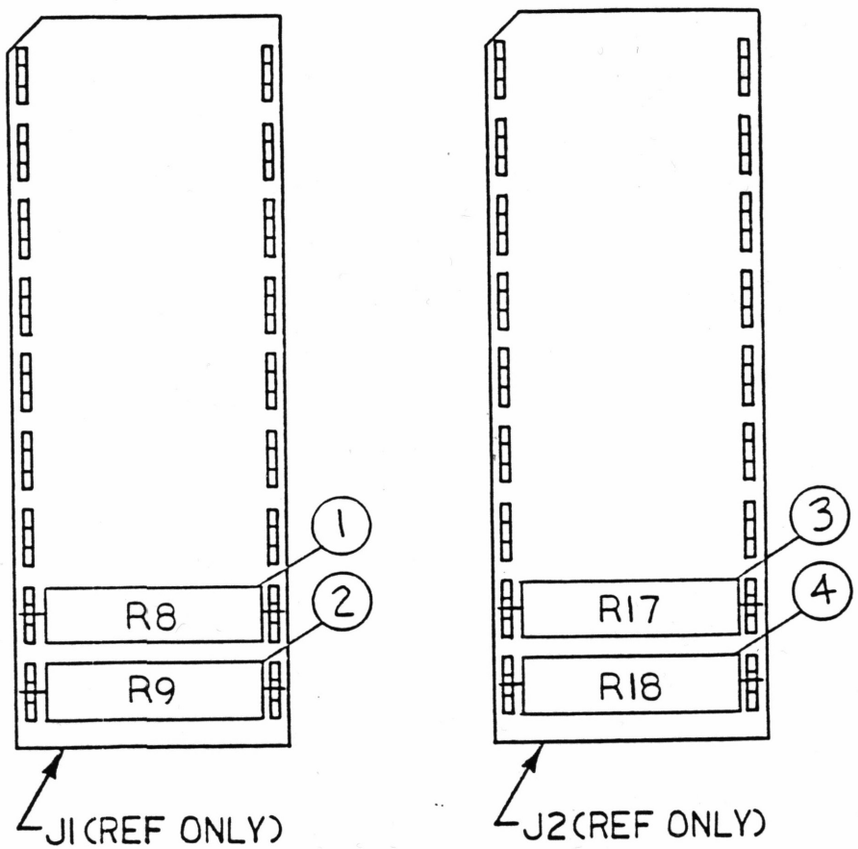
1. ALL RESISTORS IN THIS KIT ARE FACTORY-SELECTED TO ELECTRONICALLY MATCH THE OSCILLATOR IN THIS KIT PRIOR TO THIS KIT BEING FACTORY-INSTALLED IN THE INSTRUMENT. ONLY THE "NOMINAL VALUES", AND NOMINAL VALUE PART NUMBERS, ARE SHOWN ON THE PARTS LIST. THE VALUE OF A RESISTOR IN ANY ACTUAL KIT MAY DIFFER FROM THE "NOMINAL VALUE" SHOWN ON THE PARTS LIST, AND MAY DIFFER BETWEEN KITS OF THIS SAME PART NUMBER. ALL RESISTORS ARE "FIXED, METAL FILM" AND, UNLESS OTHERWISE NOTED ON THE PARTS LIST AND NEXT TO THE DRAWING CALLOUT, ALL RESISTORS ARE "1/10 WATT, ±25 PPM/DEG C" AND ARE FACTORY-SELECTED FROM MILITARY TYPE RN55E____F. FOR FIELD-REPLACEMENT OR FIELD-REPAIR OF THIS KIT, SEE "A" AND "B", BELOW.

   A. IF THE OSCILLATOR FAILS IN THE FIELD, A COMPLETE NEW KIT MUST BE FIELD-INSTALLED AFTER FIRST REMOVING FROM THE INSTRUMENT THE FAILED OSCILLATOR AND ALL RESISTORS THAT ARE PART OF THE KIT. (IT MAY BE NOTED THAT THE RESISTANCE VALUE OF A RESISTOR IN THE NEW KIT MAY BE DIFFERENT THAN THE RESISTANCE VALUE OF THE RESISTOR THAT IT IS REPLACING IN THE INSTRUMENT. THE REASON FOR THIS POSSIBLE DIFFERENCE IS DUE TO THE FACTORY-SELECTIONS MENTIONED ABOVE, AND THE RESISTOR IN THE NEW KIT MUST BE USED.)

   B. IF A RESISTOR FAILS IN THE FIELD, IT CAN BE FIELD-REPLACED BUT ONLY WITH AN EXACT DUPLICATE OF THE ONE IN THE INSTRUMENT. TO ACCOMPLISH THIS, MAINTENANCE PERSONNEL MUST BE ABLE TO IDENTIFY THE EXACT RESISTANCE VALUE OF THE FAILED RESISTOR IN THE INSTRUMENT. IF THE EXACT RESISTANCE VALUE OF THE FAILED RESISTOR CAN NOT BE DETERMINED, A COMPLETE NEW KIT MUST BE FIELD-INSTALLED AS IN "A", ABOVE.

2. RESISTORS R8, R9, R17 AND R18 (ITEMS 1 THRU 4) ARE INSTALLED WHERE SHOWN IN J1 AND J2 (ITEMS 250 AND 251 ON ASSY DRAWING 07559601).

3. FOR THE INSTALLED LOCATION OF ITEM 5 (Y1), SEE CALLOUT 6 ON ASSY DRAWING 07516202.



SEE SEPARATE PARTS LIST

FIGURE 7-63
A1A25A1A13A1, 1.9 to 6 GHz OSCILLATOR KIT
077190 REv A

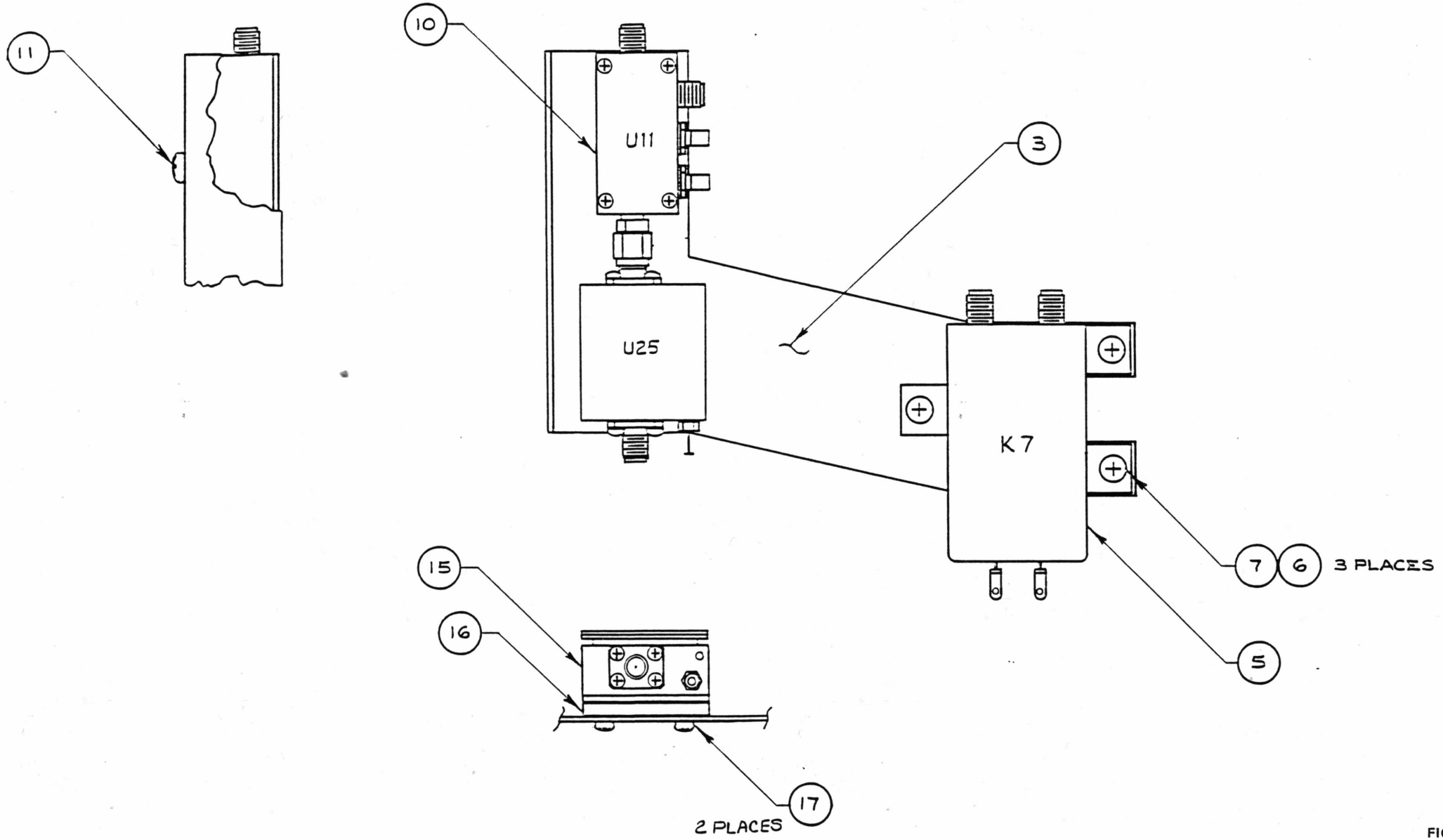


FIGURE 7-64
A1A25A1A14, RELAY AND MODULE MOUNTING
BRACKET ASSE „BLY 07580401 Rev A

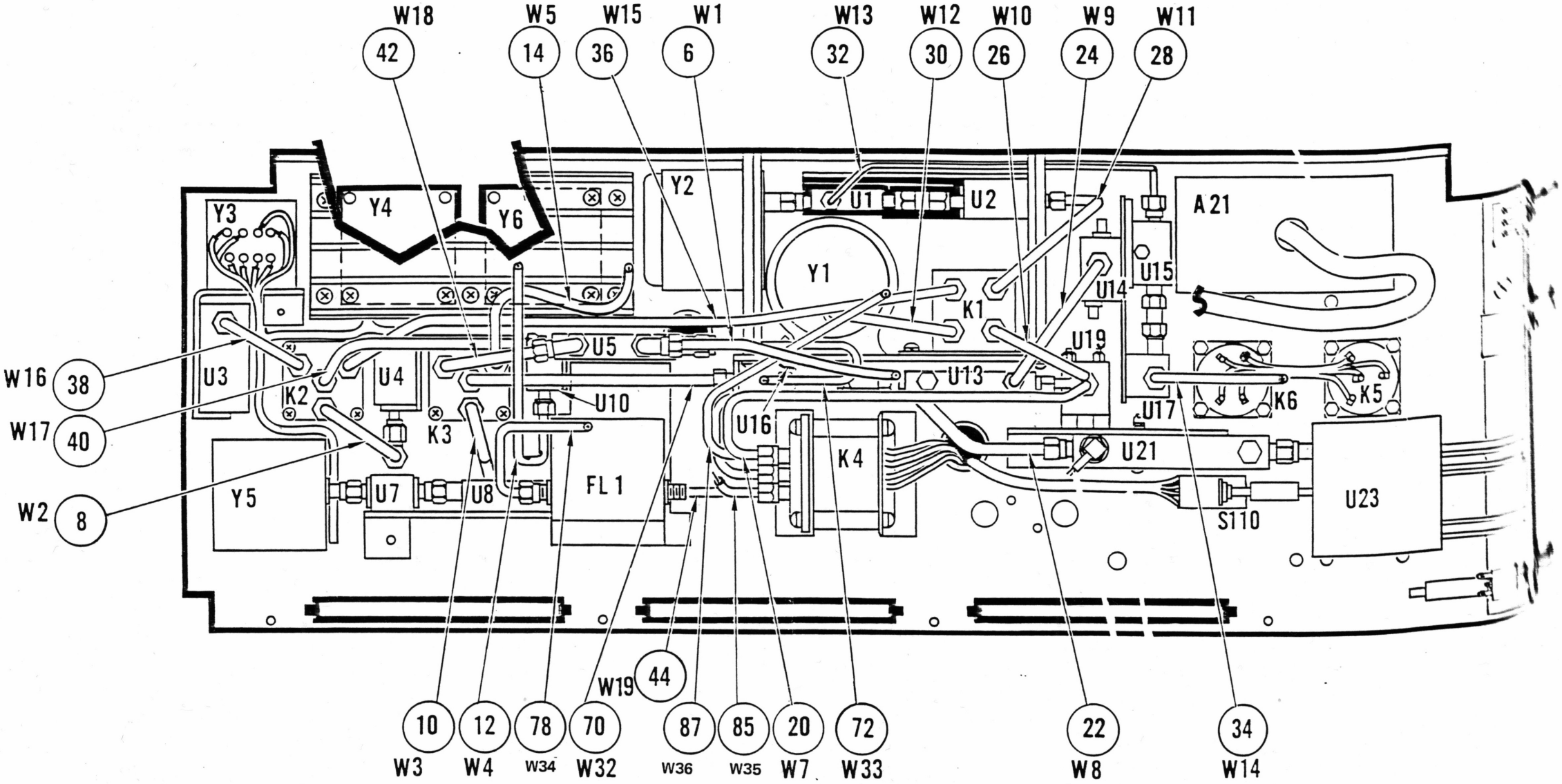


FIGURE 7-[illegible]
A1A25A1A15, MICROWAVE [illegible]
ASSEMBLY 075191 Rev [illegible]

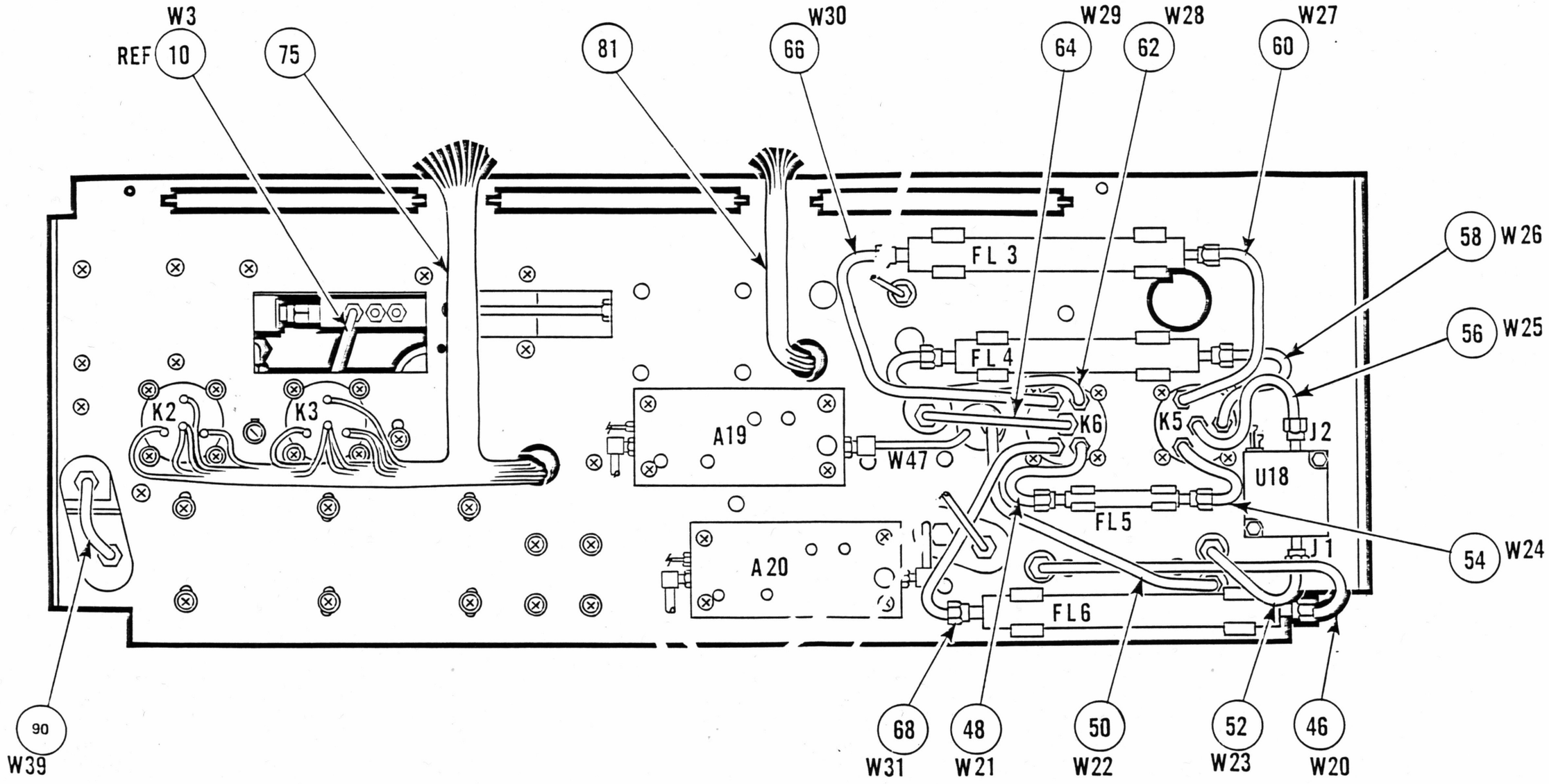


FIGURE 7-65
A1A25A1A15, MICROWAVE CHASSIS CABLING
ASSEMBLY 075191 Rev F (Sheet 2 of 3)

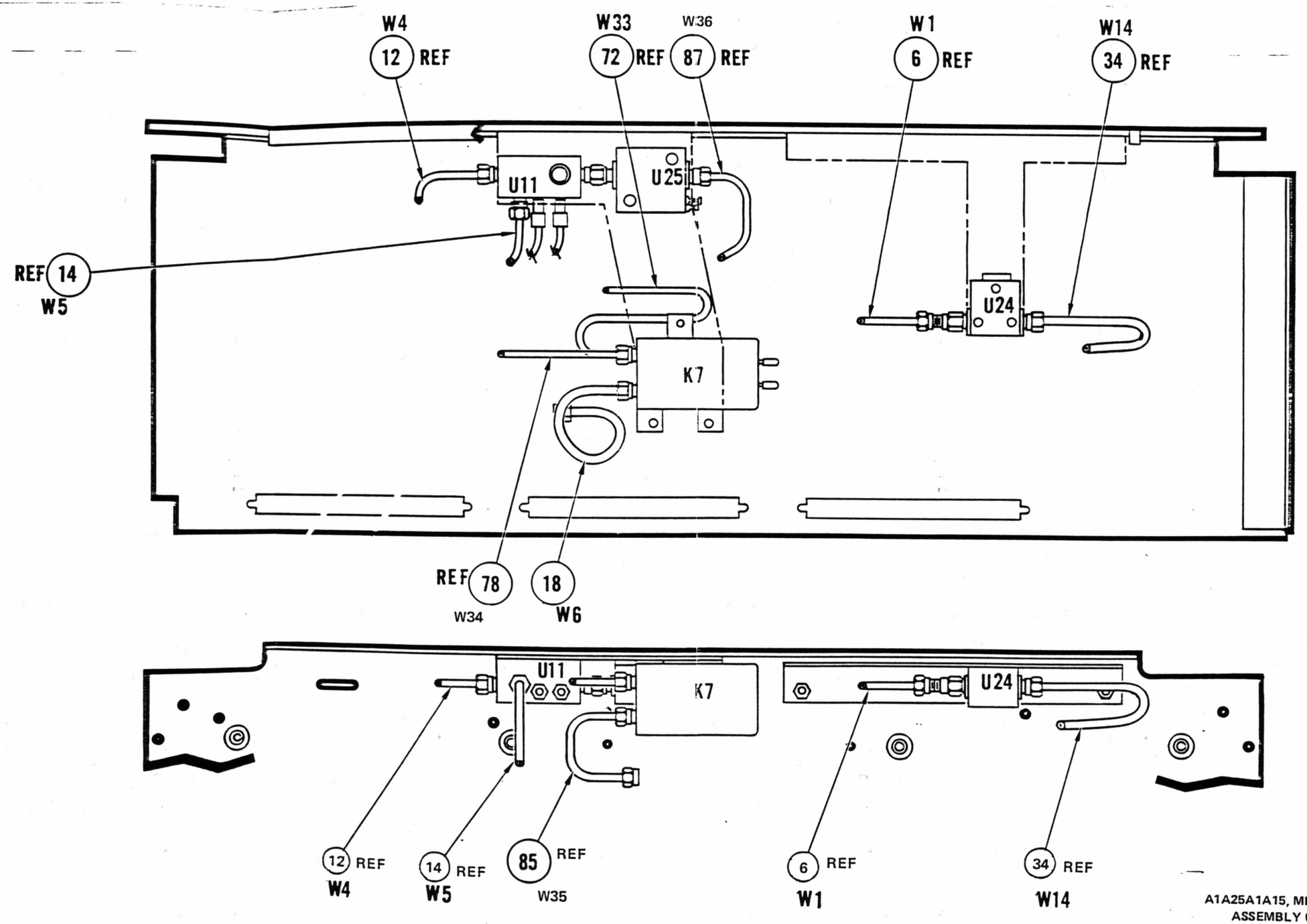


FIGURE 7-65
A1A25A1A15, MICROWAVE CHASSIS CABLING
ASSEMBLY 075191 Rev F (Sheet 3 of 3)

NOTES:

1. ALL RESISTORS IN THIS KIT ARE FACTORY-SELECTED TO ELECTRONICALLY MATCH THE OSCILLATOR IN THIS KIT PRIOR TO THIS KIT BEING FACTORY-INSTALLED IN THE INSTRUMENT. ONLY THE "NOMINAL VALUES", AND NOMINAL VALUE PART NUMBERS, ARE SHOWN ON THE PARTS LIST. THE VALUE OF A RESISTOR IN ANY ACTUAL KIT MAY DIFFER FROM THE "NOMINAL VALUE" SHOWN ON THE PARTS LIST, AND MAY DIFFER BETWEEN KITS OF THIS SAME PART NUMBER. ALL RESISTORS ARE "FIXED, METAL FILM" AND, UNLESS OTHERWISE NOTED ON THE PARTS LIST AND NEXT TO THE DRAWING CALLOUT, ALL RESISTORS ARE "1/10 WATT, ±25 PPM/DEG C" AND ARE FACTORY-SELECTED FROM MILITARY TYPE RN55E____F. FOR FIELD-REPLACEMENT OR FIELD-REPAIR OF THIS KIT, SEE "A" AND "B", BELOW.

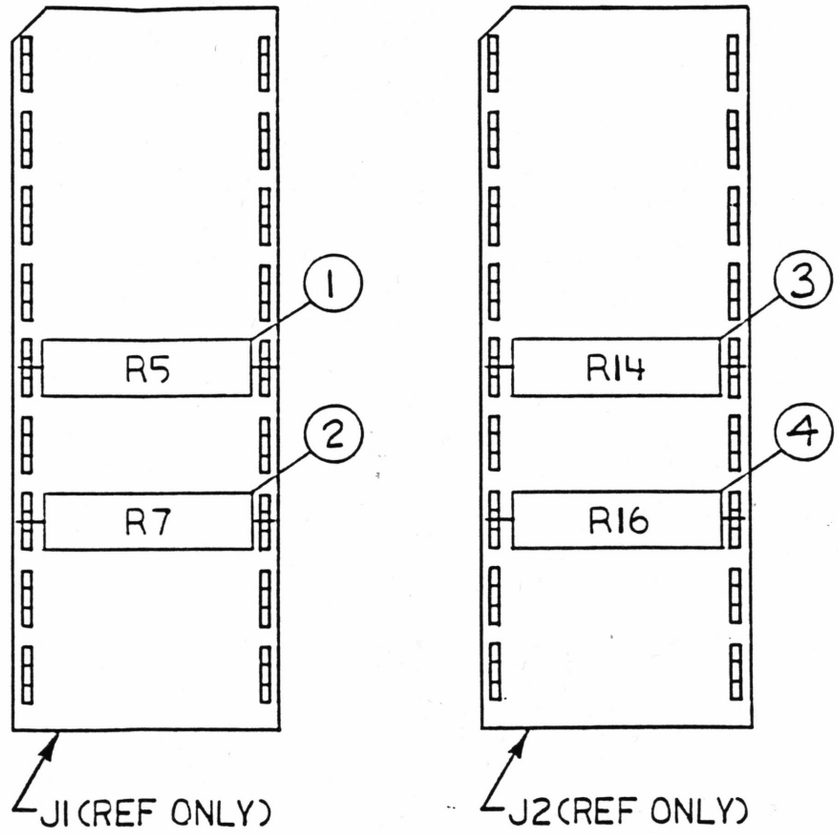
   A. IF THE OSCILLATOR FAILS IN THE FIELD, A COMPLETE NEW KIT MUST BE FIELD-INSTALLED AFTER FIRST REMOVING FROM THE INSTRUMENT THE FAILED OSCILLATOR AND ALL RESISTORS THAT ARE PART OF THE KIT. (IT MAY BE NOTED THAT THE RESISTANCE VALUE OF A RESISTOR IN THE NEW KIT MAY BE DIFFERENT THAN THE RESISTANCE VALUE OF THE RESISTOR THAT IT IS REPLACING IN THE INSTRUMENT. THE REASON FOR THIS POSSIBLE DIFFERENCE IS DUE TO THE FACTORY-SELECTIONS MENTIONED ABOVE, AND THE RESISTOR IN THE NEW KIT MUST BE USED.)

   B. IF A RESISTOR FAILS IN THE FIELD, IT CAN BE FIELD-REPLACED BUT ONLY WITH AN EXACT DUPLICATE OF THE ONE IN THE INSTRUMENT. TO ACCOMPLISH THIS, MAINTENANCE PERSONNEL MUST BE ABLE TO IDENTIFY THE EXACT RESISTANCE VALUE OF THE FAILED RESISTOR IN THE INSTRUMENT. IF THE EXACT RESISTANCE VALUE OF THE FAILED RESISTOR CAN NOT BE DETERMINED, A COMPLETE NEW KIT MUST BE FIELD-INSTALLED AS IN "A", ABOVE.

2. RESISTORS R5, R7, R14 AND R16 (ITEMS 1 THRU 4) ARE INSTALLED WHERE SHOWN IN J1 AND J2 (ITEMS 250 AND 251 ON ASSY DRAWING 0755960[illegible]).

3. FOR THE INSTALLED LOCATION OF ITEMS 5 (R37) AND 6 (R49), SEE NOTE 5 ON ASSY DRAWING 07559601. ITEM 5 (R37) IS 1/8 WATT, ±[illegible]0 PPM/DEG C.

4. FOR THE INSTALLED LOCATION OF ITEM 7 (Y2), SEE CALLOUT 35 ON ASSY DRAWING 07583801.



SEE SEPARATE PARTS LIST

FIGURE 7-66
A1A25A1A16, 4 to 8.7 GHz Y2 OSCILLATOR KIT
077191 Rev A

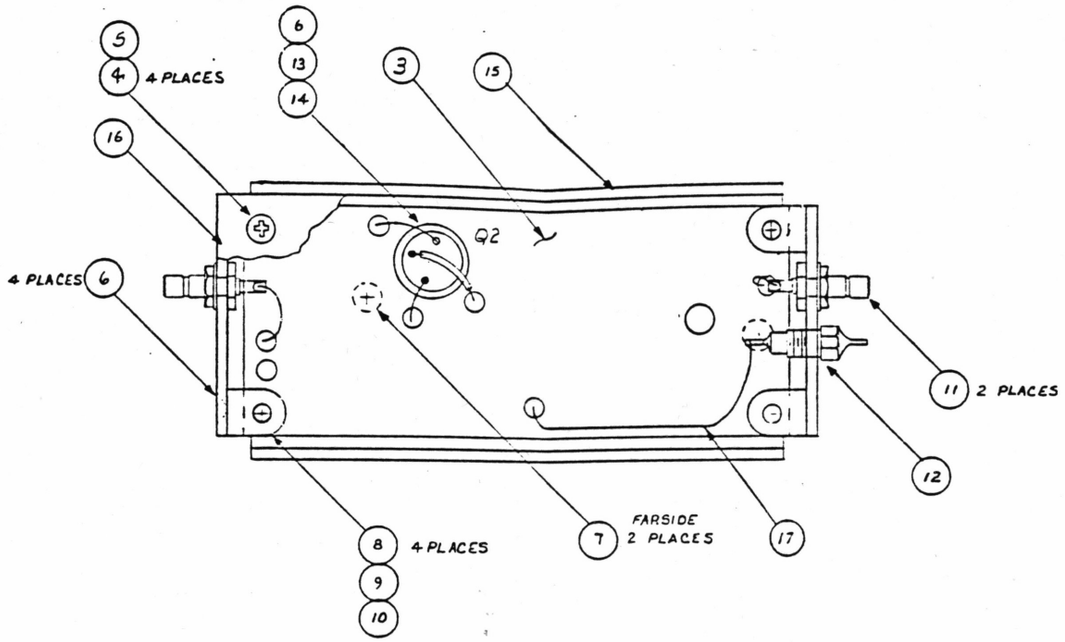


FIGURE 7-67
A1A25A1A19 and A1A25A1A20, SAMPLER DRIVER
ASSEMBLY 067711 Rev E

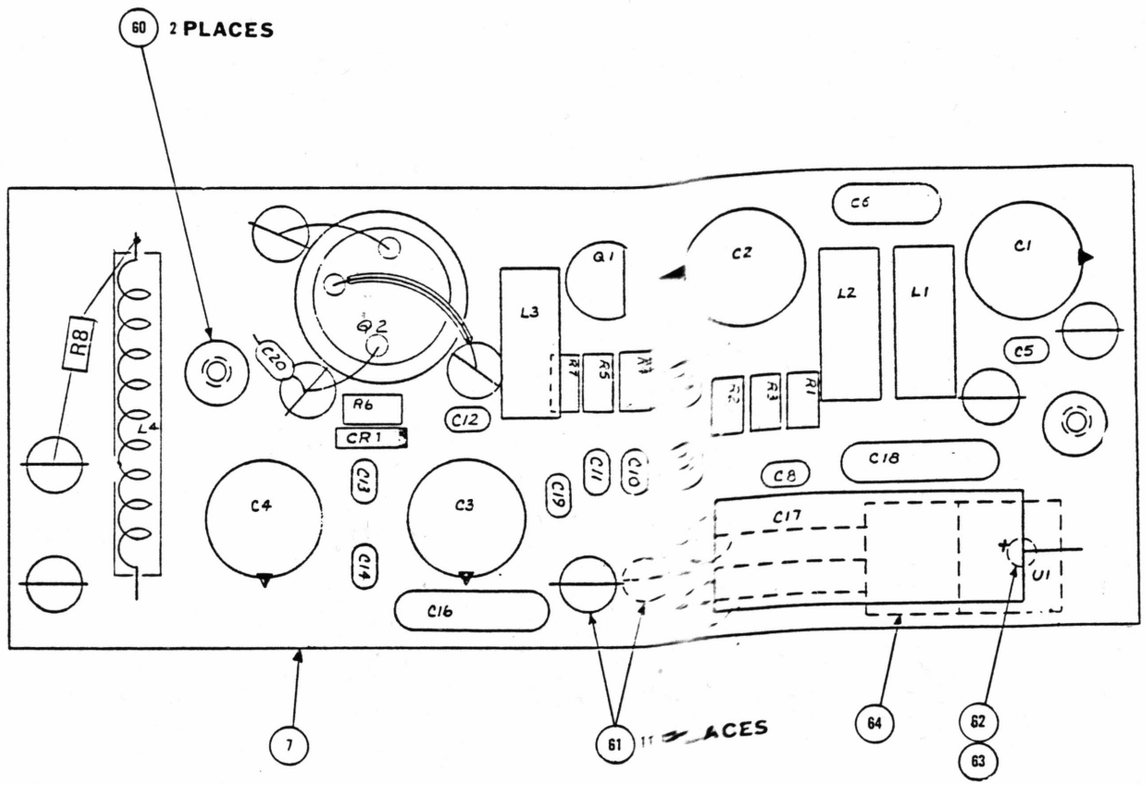
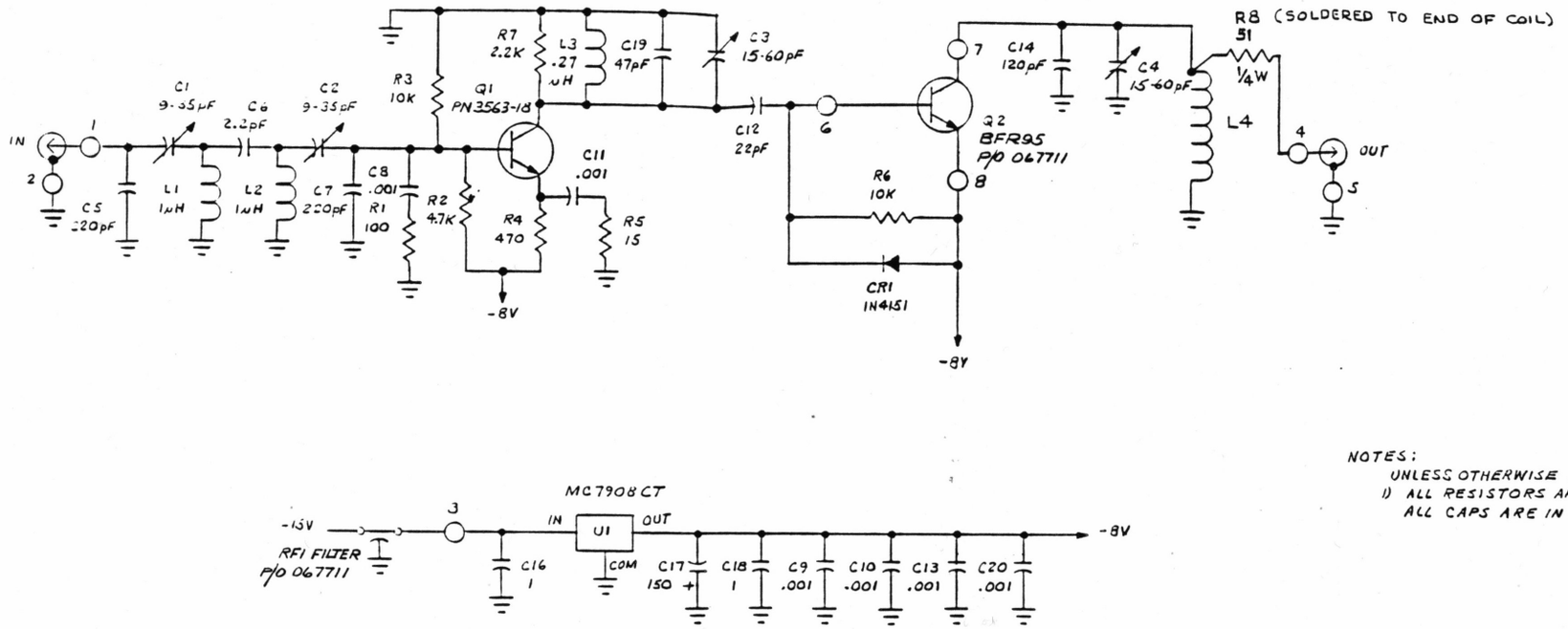


FIGURE 7-68
A1A25A1A19A1 and A1A25A1A20A1 SAMPLER
DRIVER PCB ASSEMBLY 06767301 Rev G



NOTES:
UNLESS OTHERWISE SPECIFIED
1) ALL RESISTORS ARE 1/8W 5% IN Ω
ALL CAPS ARE IN μF.

FIGURE 7-69
A1A25A1A19A1 and A1A25A1A20A1 SAMPLER DRIVER PCB SCHEMATIC 7-06767301 Rev D

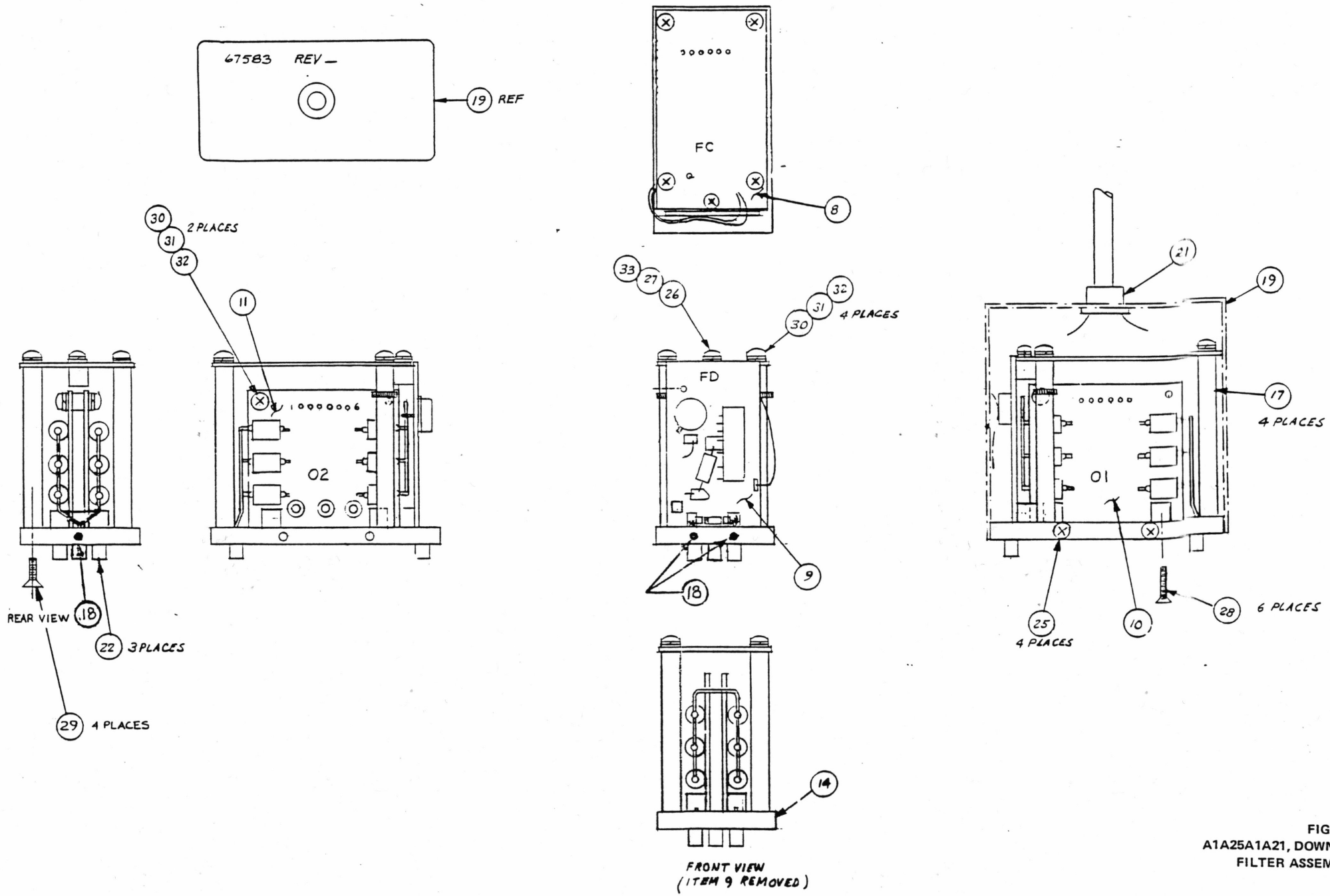
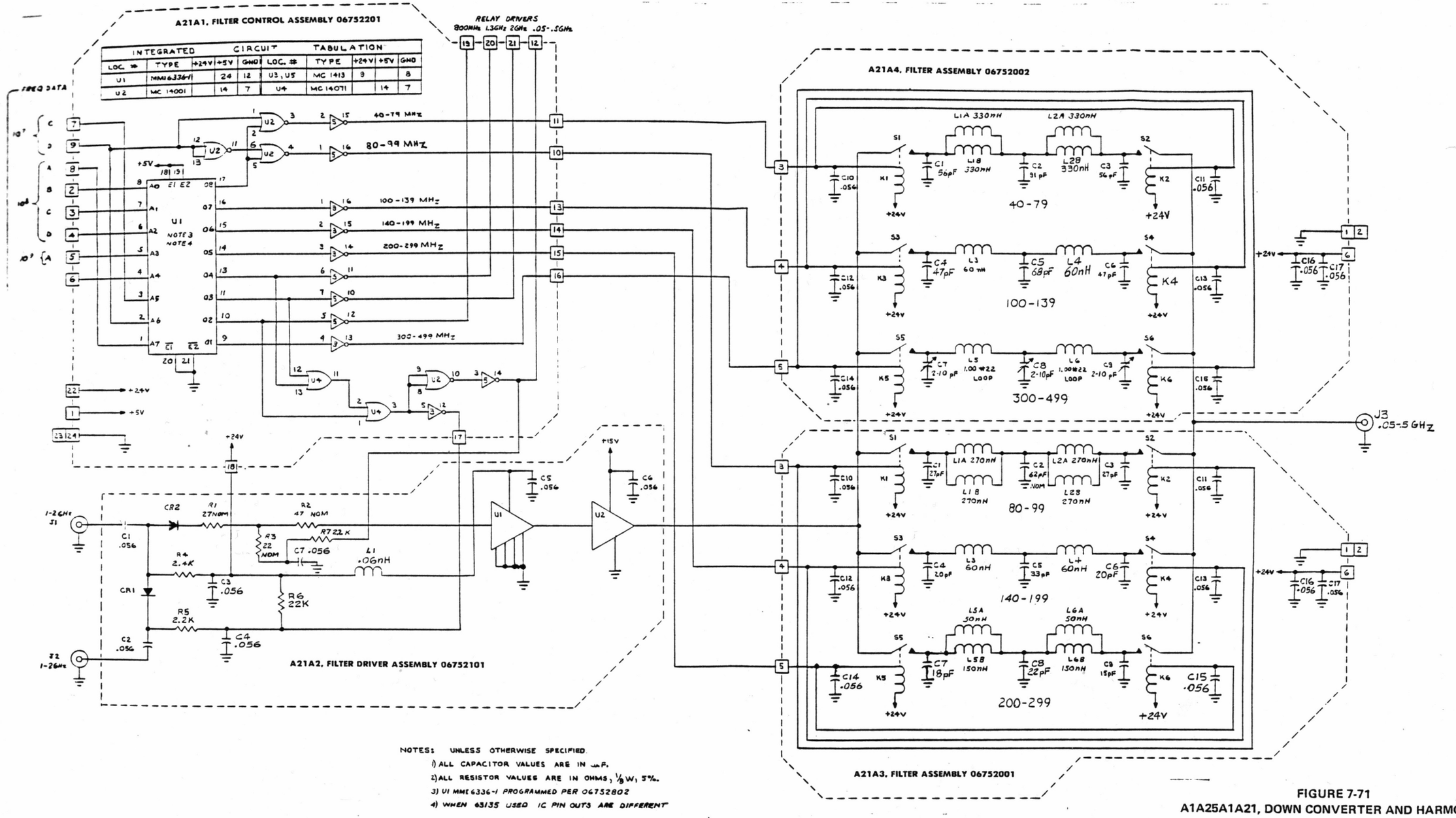


FIGURE 7-70
A1A25A1A21, DOWN CONVERTER AND HARMON
FILTER ASSEMBLY 067583 Rev F



NOTES: UNLESS OTHERWISE SPECIFIED.

1) ALL CAPACITOR VALUES ARE IN μF.
2) ALL RESISTOR VALUES ARE IN OHMS, 1/8 W, 5%.
3) U1 MMI 6336-1 PROGRAMMED PER 06752802
4) WHEN 63135 USED IC PIN OUTS ARE DIFFERENT

FIGURE 7-71
A1A25A1A21, DOWN CONVERTER AND HARMONIC FILTER SCHEMATIC 7-067583 Rev H

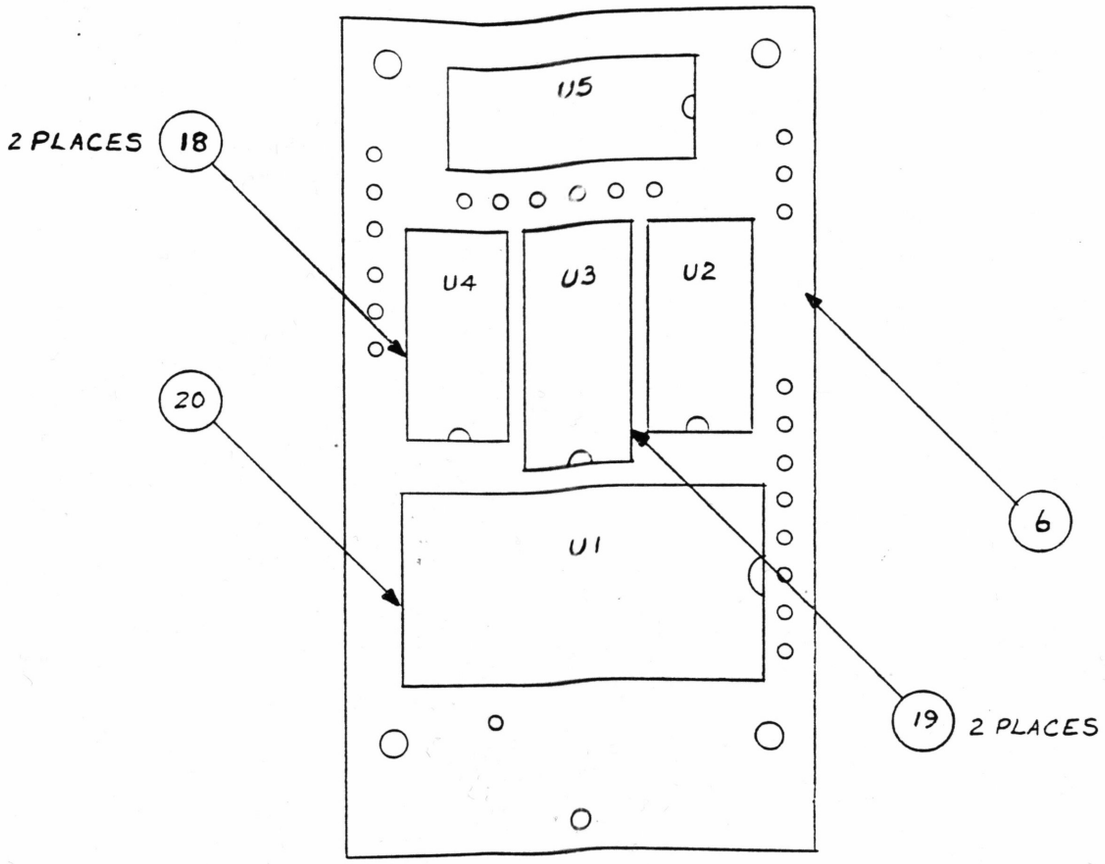


FIGURE 7-72
A1A25A1A21A1, FILTER CONTROL PCB
ASSEMBLY 06752201 Rev B

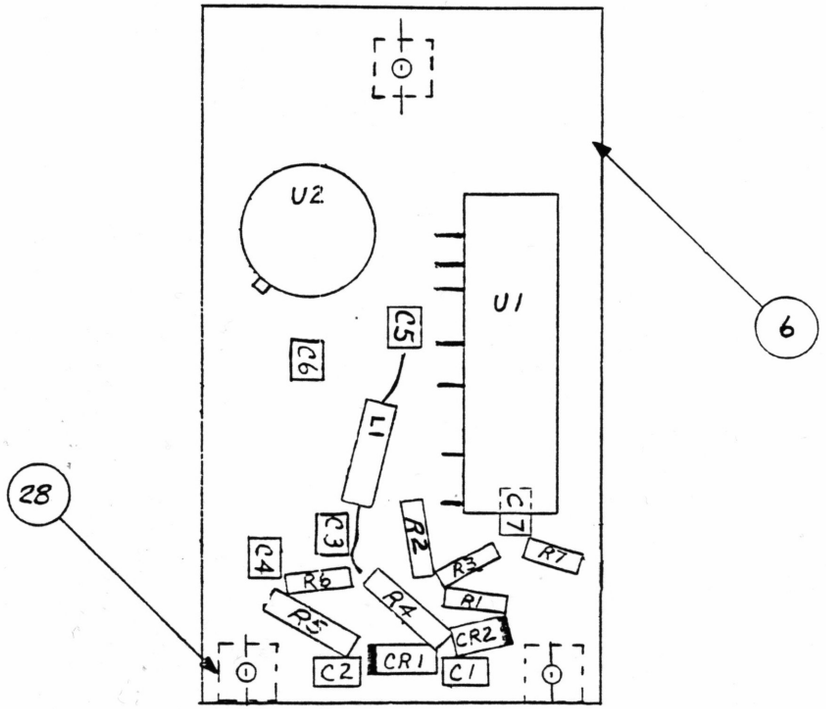
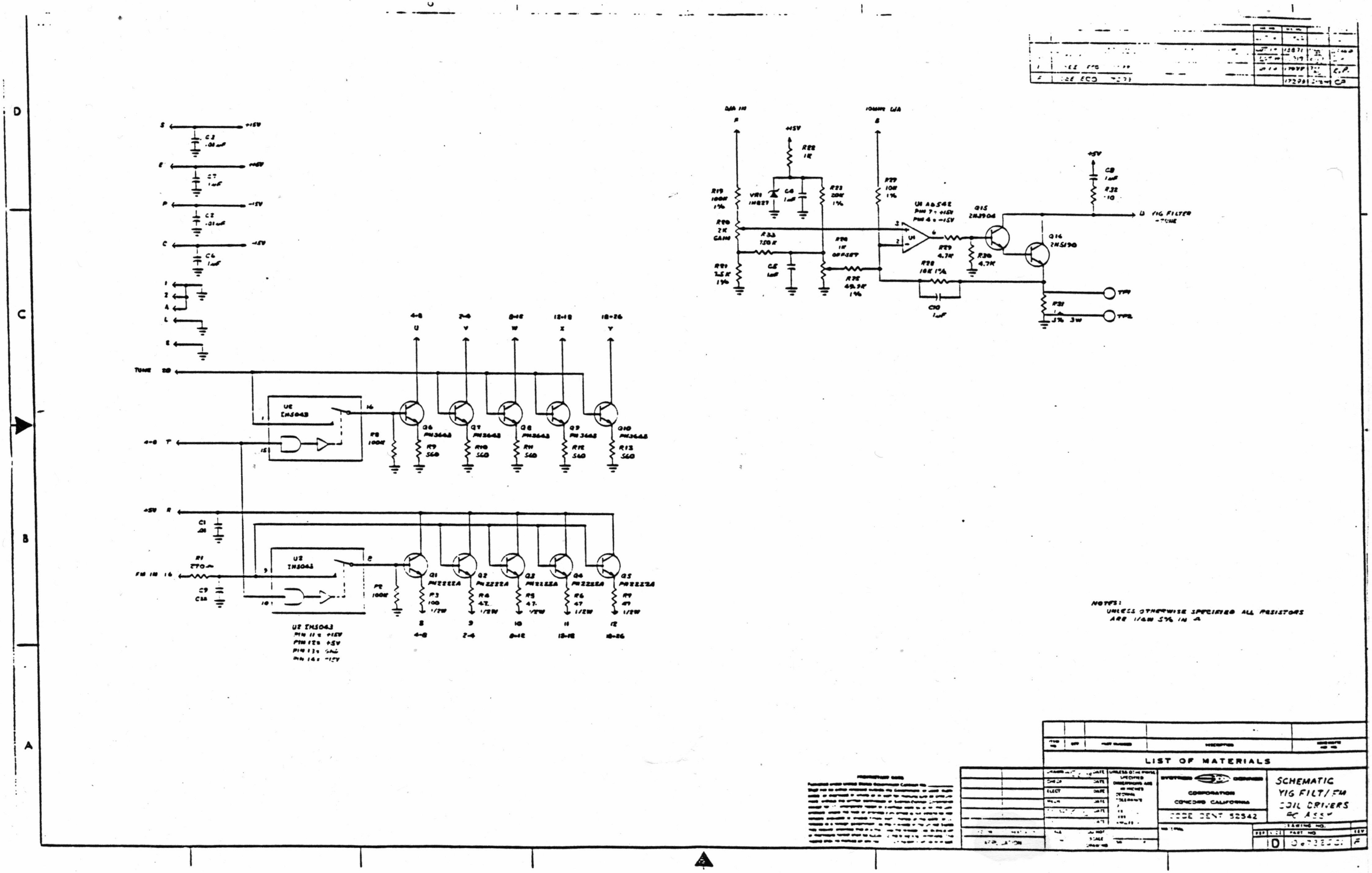
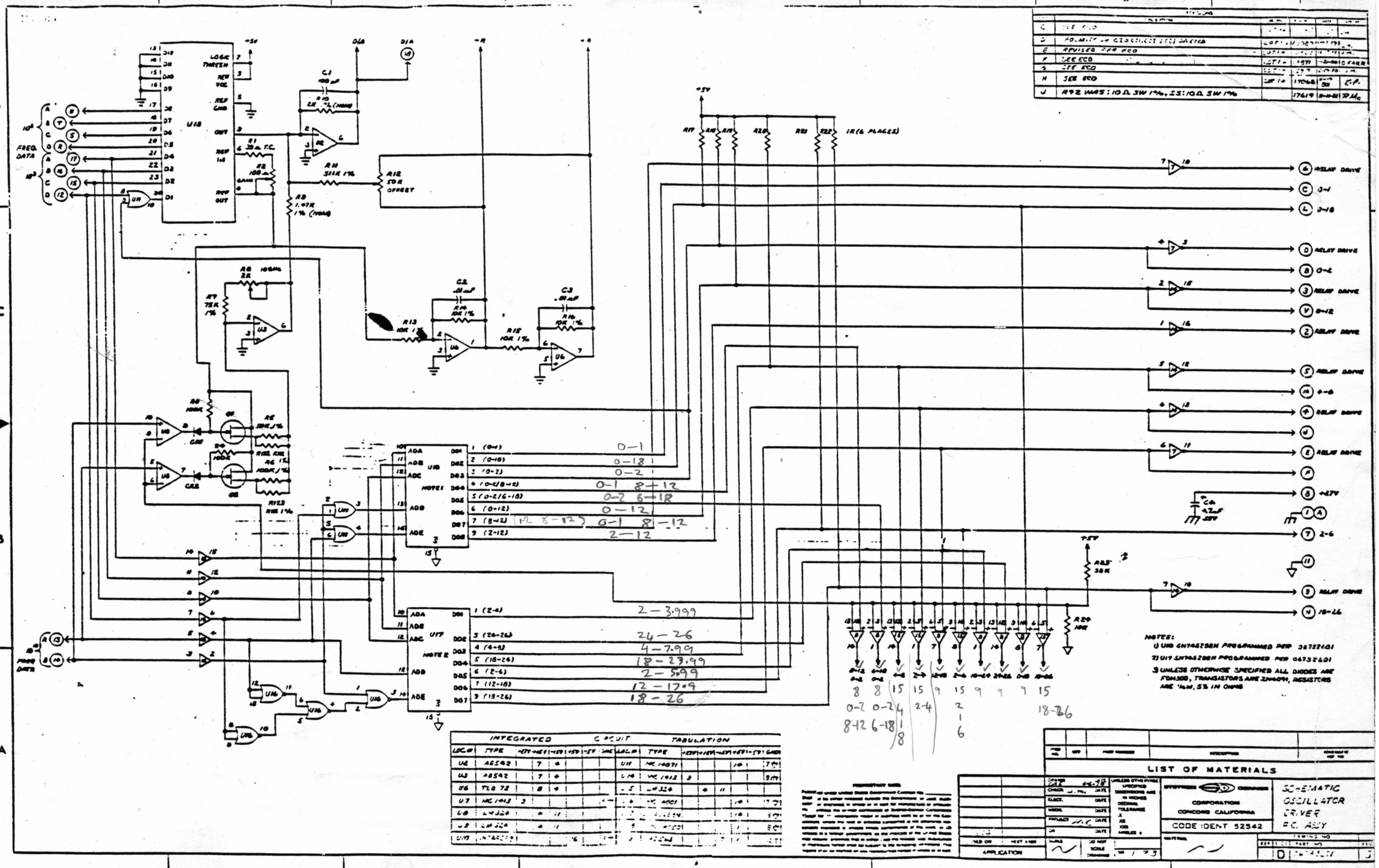
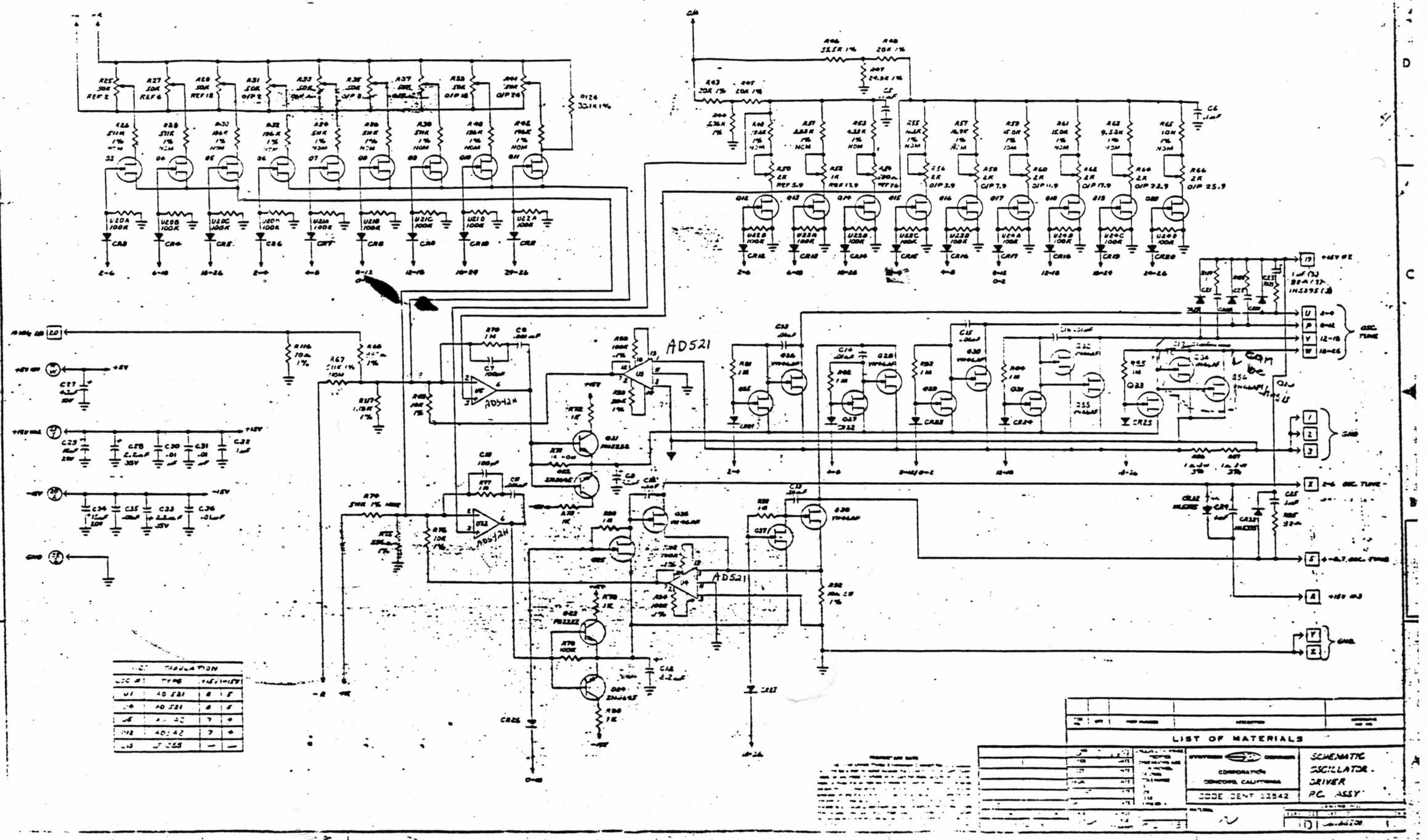


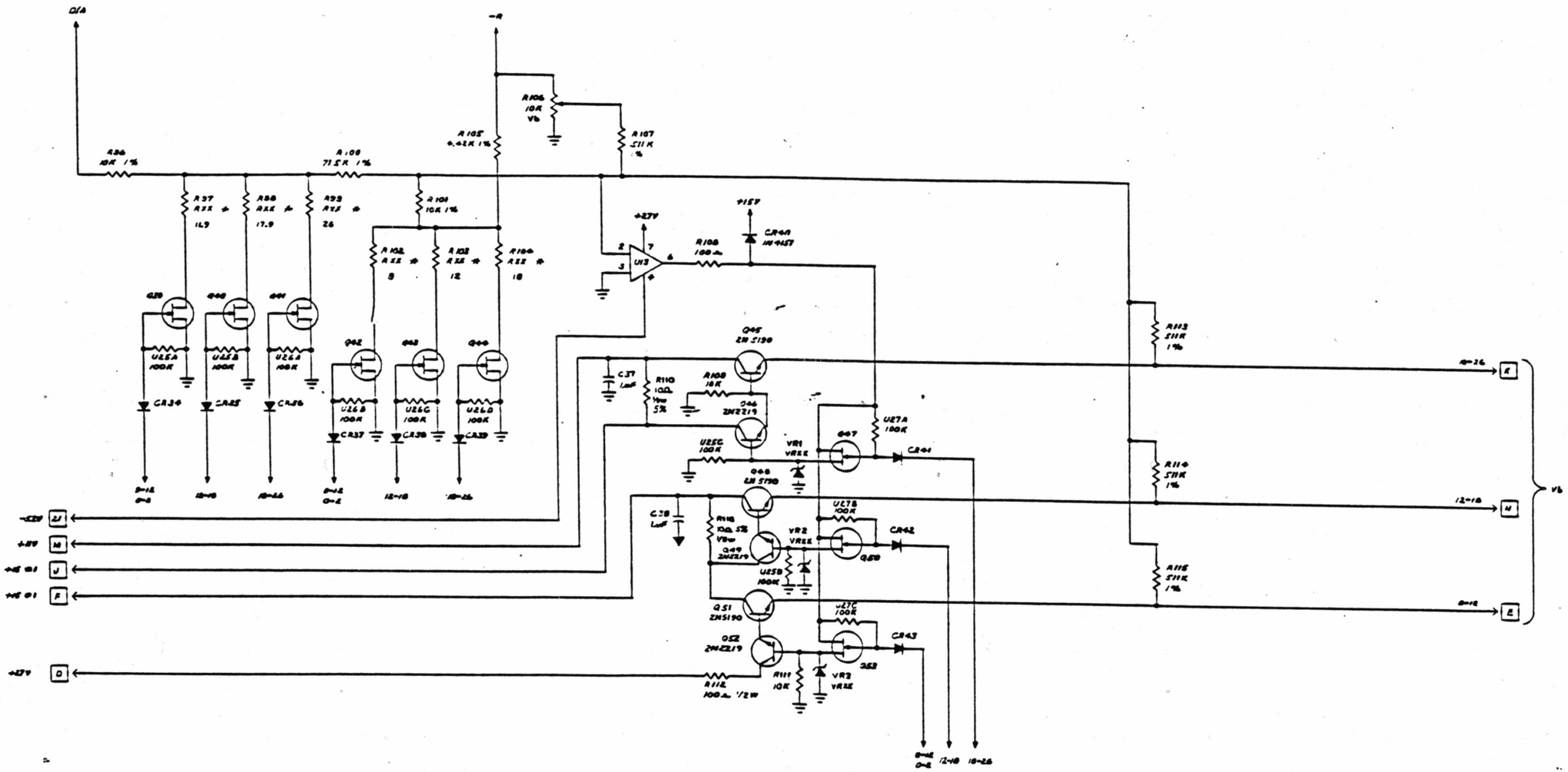
FIGURE 7-73
A1A25A1A21A2, FILTER DRIVER PCB
ASSEMBLY 06752101 Rev D



UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE 1/4W 5% IN Ω
LIST OF MATERIALS
CORPORATION
CONCORD CALIFORNIA
CODE IDENT 52542
SCHEMATIC
YIG FILT/FM
COIL DRIVERS
PC ASSY
D
F


FREQ. DATA
U18
LOGIC THRESH
REF VOL
REF GND
OUT
RNG IND
RNG OUT
+5V
C1 100 pF
R10 25K 1% (NOM)
R1 39 Ω T.C.
R2 100 Ω GAIN
R11 511K 1%
R12 50K OFFSET
R3 1.47K 1% (NOM)
U1A
U3
R8 2K
R7 75K 1%
C2 .01 mF
R14 10K 1%
R13 10K 1%
U6
R15 10K 1%
C3 .01 mF
R16 10K 1%
U6
R4 100K
Q1
R5 100K 1%
R24 100K
Q2
R6 100K 1%
R23 100K 1%
U4B
U4A
U5A
U5B
U5C
U5D
U6A
U6B
U6C
U6D
U18
NOTE 1
U17
NOTE 2
ADA
ADB
ADC
ADD
ADE
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
1 (0-1)
2 (0-18)
3 (0-2)
4 (0-2/8-12)
5 (0-2/6-18)
6 (0-12)
7 (8-12)
9 (2-12)
1 (2-4)
3 (24-26)
4 (4-8)
5 (18-24)
6 (2-6)
7 (12-18)
9 (18-26)
0-1
0-18
0-2
0-1 8-12
0-2 6-18
0-12
0-1 8-12
2-12
2-3.999
24-26
4-7.99
18-23.99
2-5.99
12-17.99
18-26
R17 10K
R18 10K
R19 10K
R20 10K
R21 10K
R22 10K
1R (6 PLACES)
+5V
R25 30K
R26 10K
G1 G2 G3 G4 G5 G6 G7 G8 G9 G10
8 8 15 15 9 15 9 9 9 15
0-2 0-24 2-4 2 1 6
8-12 6-18 1 8
18-26
C4 4.7 mF 25V
+27V
RELAY DRIVE
0-1
0-2
0-12
0-8
2-6
18-26
NOTES:
1) U18 SN74S288N PROGRAMMED PER 06732401
2) U17 SN74S288N PROGRAMMED PER 06732401
3) UNLESS OTHERWISE SPECIFIED ALL DIODES ARE FDH300, TRANSISTORS ARE 2N4091, RESISTORS ARE 1/4W, 5% IN OHMS
INTEGRATED CIRCUIT TABULATION
LOC.# TYPE +5V +15V -15V -5V SPARE GATES
U2 AD562 7 4 1
U3 AD542 7 4 1
U6 TL072 8 4 1
U7 MC1413 3 7
U8 LM324 4 11 1
U9 LM324 4 11 1
U10 SN74S288N 16 1
U11 MC14071 14 1
U16 MC1413 3 7
U5 LM324 4 11 1
U4 MC4001 14 1
U1 LM324 4 11 1
U12 LM324 4 11 1
U13 MC4001 14 1
LIST OF MATERIALS
SCHEMATIC OSCILLATOR DRIVER P.C. ASSY
CORPORATION CONCORD CALIFORNIA
CODE IDENT 52542
APPLICATION
DRAWING NO 06732401
SIZE D
REV J


AD521
AD524
AD521
+15V
-15V
+5V
GND
OSC. TUNE
GND
+15V
-15V
+5V
GND
OSC. TUNE
GND
+15V
GND
LIST OF MATERIALS
SCHEMATIC OSCILLATOR-DRIVER P.C. ASSY
CODE IDENT 12542



LIST OF MATERIALS

SCHEMATIC OSCILLATOR DRIVER PC ASSY

CONCORD CALIFORNIA

CODE IDENT 80542

D

J	SEE ECO
K	SEE ECO
K1	POLARITY OF C4 CORRECTED
L	SEE ECO. Q32 DELETED
M	R92 WAS: 10Ω 3W, IS: 10Ω 5W

ADD VR2, VR1F FROM Q49 BASE (B) TO GND AT Q42 SOURCE (S) ON BACK SIDE OF PC BD, CATHODE ON Q49-B (WRAP LEADS)

INSULATE LEADS WHERE REQ'D TO PREVENT SHORTING TO TRACES

ADD VR1, VR2 FROM Q46 BASE (AT FEED THRU BETWEEN R103 & R104) TO GND (AT Q44 SOURCE) ON BACK SIDE OF PC BD, CATHODE IN FEED THRU. (WRAP #30GE LEAD TO Q44-S)

VR1F 10K

331

327 42 PLACES

322 2 PLACES (U1 & U6)

332 60 PLACES FARSIDE

ADD R110 FROM COLLECTOR Q45 TO Q46 & R118 FROM Q48 COLLECTOR TO Q49 COLL. INSULATE LEADS TO PREVENT SHORTS (BACK SIDE)

336 3 PLACES

339

344

ADD C27 1uF BETWEEN Q45 COLLECTOR AND GND. TO R87 (GND) ON BACK SIDE OF BD WRAP LEAD AND INSULATE TO PREVENT SHORTS.

ADD C28 1uF FROM Q51 COLLECTOR TO R87 LEAD (GND) ON BACK SIDE OF PC BD (WRAP LEAD TO R87) INSULATE LEADS IF REQ'D TO PREVENT SHORTS

USE THERMALL COMPOUND ON BOTH SIDES REF UNDER Q54 & Q55 (2 PLACES)

332 REF

345

350

335 (5PL)

R120 B2A (UNDER R87)

R121 B2A (UNDER RB6)

R119 B2A (UNDER RB6)

336 7 PLACES

339

345 2 PLACES

INSULATED JUMPER (22 GA. BUS WIRE) FROM U20 CENTER PIN TO R92 ON FARSIDE OF BD WRAP JUMPER ON COMPONENT LEADS

ALL UNLABELED TRANSISTORS ARE 2N4904.

323 2 PLACES (U17 & U18)

324

ALL UNLABELLED DIODES ARE FDH300.

345 REF FAR SIDE

339 REF

356 REF

Q32, Q34, Q52, Q54, Q55, Q35

6

342

343 METAL CLAD SURFACE TO BE IN CONTACT WITH SPACER

338

348

PROPRIETARY DATA

LIST OF MATE

UNLESS OTHERWISE SPECIFIED

DIVERSITECH

K	SEE ECO
K1	POLARITY OF C9 CORRECTED
L	SEE ECO. Q8E DELETED
M	R92 WAS: 10Ω 3W, IS: 10Ω 5W

ADD VR2, VR11 FROM Q49 BASE (B) TO GND AT Q42 SOURCE (S) ON BACK SIDE OF PC BD, CATHODE ON Q49-B (WRAP LEADS)

INSULATE LEADS WHERE REQ'D TO PREVENT SHORTING TO TRACES

ADD VR1, VR22 FROM Q46 BASE (AT FEED THRU BETWEEN R103 & R104) TO GND (AT Q44 SOURCE) ON BACK SIDE OF PC BD, CATHODE IN FEED THRU. (WRAP ANODE LEAD TO Q44-S)

VR11 10K

331

327 42 PLACES

322 2 PLACES (U1 & U4)

332 10 PLACES FARSIDE

ADD R110 FROM COLLECTOR Q45 TO GATE OF R118 FROM Q48 COLLECTOR TO Q49 COLL. INSULATE LEADS TO PREVENT SHORTS (BACK SIDE)

336 3 PLACES

339

344

ADD C37 1uF BETWEEN Q45 COLLECTOR AND GND. TO R87 (GND) ON BACK SIDE OF BD WRAP LEAD AND INSULATE TO PREVENT SHORTS.

ADD C28 1uF FROM Q61 COLLECTOR TO R87 LEAD (GND) ON BACK SIDE OF PC BD (WRAP LEAD TO R87) INSULATE LEADS IF REQ'D TO PREVENT SHORTS

332 REF

345

350 USE THERMAL COMPOUND ON BOTH SIDES REF UNDER Q54 & Q55 (2 PLACES)

335 (5PL)

R120 82Δ (UNDER R87)

R121 82Δ (UNDER R84)

R119 82Δ (UNDER R84)

336 7 PLACES

339

345 2 PLACES

INSULATED JUMPER (22 GA. BUS WIRE) FROM U20 CENTER PIN TO R92 ON FARSIDE OF BD WRAP JUMPER ON COMPONENT LEADS

ALL UNLABELED TRANSISTORS ARE 2N4901.

323 2 PLACES (U17 & U18)

324

ALL UNLABELED DIODES ARE FDH300.

348 REF FAR SIDE

339 REF

336 REF

6

342

343 METAL CLAD SURFACE TO BE IN CONTACT WITH SPACER

336

348

LIST OF MATE

PROPRIETARY DATA

SYSTRON CORPORATION